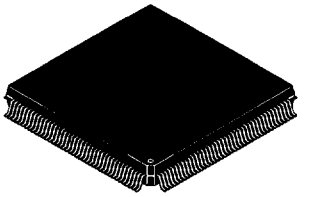
MCD270

Technical Summary

IMPEG Integrated Video and Audio Decoder



FU SUFFIX
QFP PACKAGE
CASE 1007–01

ORDERING INFORMATION
MCD270FU QFP

This technical summary provides a brief description of the MCD270 IMPEG Integrated Video and Audio Decoder. A complete data sheet for the MCD270 is available and can be ordered from your local Motorola sales office. The order number is MCD270/D.

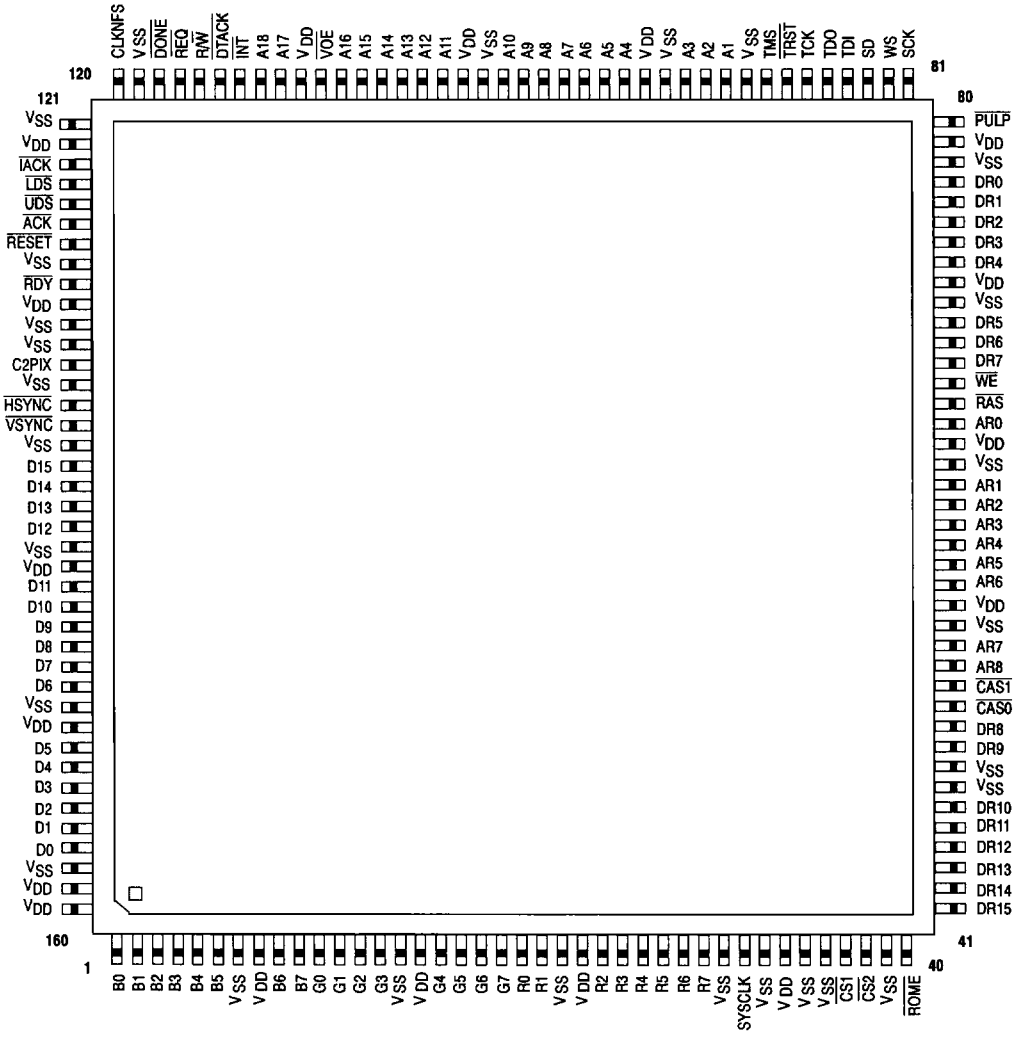
The MCD270 is a single chip MPEG1 Audio and Video Decoder, requiring the addition of only a single 4 Mbits DRAM and appropriate DACs to provide full MPEG1 decoding for consumer multimedia applications such as CD–i, CD–Karaoke, Video–CD, and Video–On–Demand type services. The main features of the device are as follows:

- Direct Interface for MC68000 Bus Compatible Devices, with DMA and Interrupt Capability
- Direct Drive of 24–Bit Triple Video DACs Such as the MC44200
- Direct Drive of 16– and 18–Bit Stereo Audio DACs via I^2S or Sony Formats
- Direct Drive of 256K x 16 DRAM for Video and Audio Buffering and Frame Reconstruction
- 11.2896 MHz, 16.9344 MHz, or 33.8688 MHz CD Clock Input for Generation of 90 kHz MPEG System and Audio Clocks
- Decodes MPEG System Layer to Allow Channel Selection, Buffer Control, and Perform Correct Audio/Video Synchronization
- Decodes 24, 25, or 30 Hz MPEG1 Constrained Parameter Video Streams and Outputs Digital 24–Bit RGB at PAL or NTSC Rates
- Capable of Decoding MPEG1 Video at Bit Rates of up to 5 Mbits Per Second
- Decodes Layer I or II MPEG1 Audio Streams, All Bit Rates, All Modes, 44.1 kHz Sample Rate
- Decodes Either Single Multiplexed ISO11172 Streams or Dual ISO11172 Streams as in CD–i, CD–Karaoke, and Video–CD
- Implements All Extra CD–i Functionality such as Windowing, Still Picture Mode, and Audio Attenuation Control
- 160–Pin Plastic Quad Flat Pack

NOTE: Supply of this Video–CD IC does not convey an implied license under any patent right to use this IC in any Video–CD application.

CD–i is a registered trademark of Philips Consumer Electronics.

PIN ASSIGNMENT



GENERAL

Motion Picture Expert Group 1 (MPEG1) is an ISO standard for the compression of digital video and associated audio. In particular MPEG1 defines a bit stream for compressed video and audio optimized for a data rate of 1.5 Mbps. This bandwidth, which is the data rate of (uncompressed) audio CDs, delivers VHS quality video and CD quality audio.

The defined standard consists of three parts; video, audio, and systems. The video and audio parts define the compression of the video and audio components, and the systems part defines the integration of the audio and video streams with proper timestamping to allow their synchronization.

The detailed specifications are contained in the following ISO standards:

- ISO 11172–1, MPEG1–System
- ISO 11172–2, MPEG1–Video
- ISO 11172–3, MPEG1–Audio

MPEG1 is the coding/compression standard that is specified for the Full Motion Extensions to CD–i and for CD–Bridge disc formats such as CD–Karaoke and Video–CD. MPEG2 and MPEG4 are not applicable and all further references to MPEG in this document refer specifically to MPEG1.

VIDEO

MPEG1 Video uses a combination of transform coding and motion compensation to exploit the spatial and the temporal redundancy present in video sequences, which (depending on the resolution of the original sequence) gives compression ratios of around 25:1. MPEG1 is a frame rather than a field based compression scheme, the frames being Intra, Predicted, or Bidirectionally predicted. Although the full specification of MPEG1 allows for high bit rates and large frame sizes, a constrained parameter stream is specified, which allows a decoder to be designed for low–cost consumer applications. CD–i and CD–Bridge formats use a constrained parameter stream, but CD–i has some extra features supported by the MCD270 which allow further windowing of video after the MPEG decoding. In addition, the MCD270 supports the CD–i still picture mode based on larger size MPEG1 frames than the constrained parameter stream allows.

AUDIO

MPEG1 Audio uses sub–band coding with dynamic bit–allocation based on a psychoacoustic model to attain compression ratios of up to 8:1 without noticeable degradation in quality when compared to CD–DA. There are three types of coding that MPEG1 Audio allows, termed layers I–III. These give approximately 4:1, 6:1, and 8:1 compression with a corresponding increase in the level of decoding complexity. Since Layer III is significantly more complex than the other two layers, the MCD270 supports only layers I and II as required by CD–i and CD–Bridge formats. The coded MPEG Audio stream also specifies the output sample rate of the decoded audio, which, although 32 kHz, 44.1 kHz, and 48 kHz are allowed within the full MPEG1 standard, is constrained to 44.1 kHz in the MCD270 as specified for CD–i and CD–Bridge formats.

SYSTEM LAYER

The MPEG System layer contains information needed for decoder buffer control, audio/video synchronization and channel demultiplexing. In CD–i and CD–Bridge discs, MPEG data is stored on the disc in separate audio and video sectors, each of which has its own MPEG System layer associated with it. This is in contrast to a conventional MPEG stream in which the audio and video are multiplexed into the same single ISO11172 stream. The MCD270 will handle either form of multiplexing.

In all CD–i and CD–Bridge MPEG streams, the system_audio_lock_flag is set, indicating that there is a constant rational relationship between the audio sample rate and the system clock frequency. Thus, MCD270 audio decoder timing (i.e., the 44.1 kHz output rate) must be locked to the CD drive when playing real–time files. This ensures correct input buffer operation without requiring the skipping or duplicating of samples, which would result in significant degradation of sound quality. Video is then locked to audio by means of an on–chip 90 kHz MPEG System Clock which is also locked to the CD drive clock.

Figure 1 illustrates a typical MPEG1 video and audio decoder.

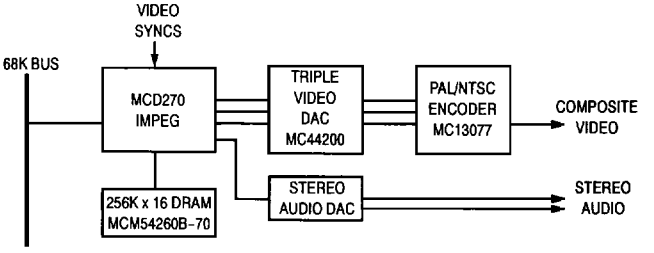
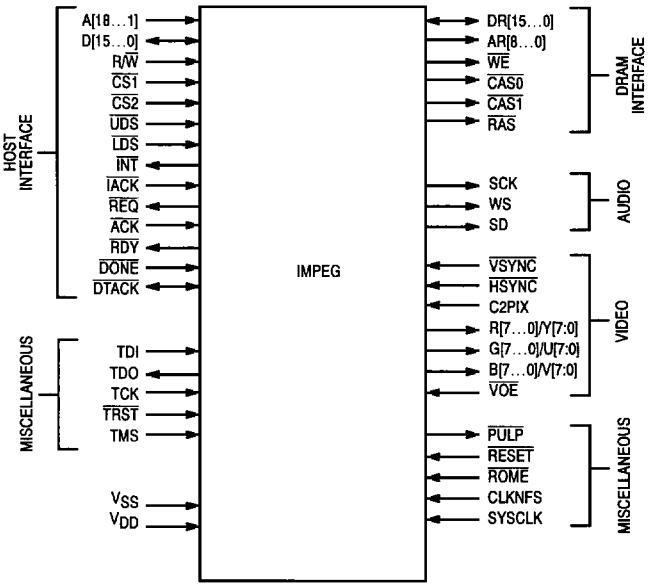


Figure 1. Typical MPEG1 Video and Audio Decoder

PIN DESCRIPTION



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PIN DESCRIPTIONS

Host Interface

Mnemonic	Type	Name and Function
A[18 ... 1]	I	Address bus.
D[15 ... 0]	B	Bidirectional databus.
R/$\overline{W}$	I	Read/$\overline{Write}$. Direction for data transfer.
$\overline{CS1}$	I	Chip select 1. Active LOW. Used for access of all audio/video related registers. Allows only word access.
$\overline{CS2}$	I	Chip select 2. Active LOW. Used for random access of the DRAM. Allows both word and byte access.
$\overline{UDS}$	I	Upper datastrobe. Active LOW. Used to address the upper byte [D15 ... D8] of a word.
$\overline{LDS}$	I	Lower datastrobe. Active LOW. Used to address the lower byte [D7 ... D0] of a word.
$\overline{INT}$	O	Interrupt request. Active LOW. Open drain output.
$\overline{IACK}$	I	Interrupt acknowledge. Active LOW.
$\overline{REQ}$	O	DMA transfer request. Active LOW. Open drain output.
$\overline{ACK}$	I	DMA acknowledge. Active LOW. Indicates that the bus is free for a DMA access.
$\overline{RDY}$	O	DMA ready. Active LOW. Indicates that the IMPEG has read data from the data bus. (Active pullup.)
$\overline{DONE}$	I	DMA done. Active LOW. Indicates that the current transfer cycle is the last cycle of a burst.
$\overline{DTACK}$	B	Data transfer acknowledge. Active LOW. During normal host access, $\overline{DTACK}$ is an output indicating that data has been put on (read cycles) or read from (write cycles) the data bus. (Active pullup.) During DMA, $\overline{DTACK}$ is an input indicating that the memory has put data on the data bus.

Video Interface

Mnemonic	Type	Name and Function
R[7 ... 0]/Y[7:0]	O	8 bit wide Red (RGB mode) or Y (YUV mode) output.
G[7 ... 0]/U[7:0]	O	8 bit wide Green (RGB mode) or U (YUV mode) output.
B[7 ... 0]/V[7:0]	O	8 bit wide Blue (RGB mode) or V (YUV mode) output.
VOE	I	Video output enable. Enables or tristates the RGB outputs; polarity defined by a host writeable register bit.
C2PIX	I	Pixel clock of twice the pixel frequency.
$\overline{\text{HSYNC}}$	I	Video line synchronization.
$\overline{\text{VSYNC}}$	I	Video vertical synchronization signal.

Audio Interface

Mnemonic	Type	Name and Function
SCK	O	Output sample clock of 2.8224 MHz (locked to CD clock).
WS	O	Wordselect. For I^2S format LOW indicates left channel, HIGH indicates right channel. For Sony format LOW indicates right channel and HIGH indicates left channel.
SD	O	Data output (MSB first).

DRAM Interface

Mnemonic	Type	Name and Function
DR[15 ... 0]	B	16 bits bidirectional DRAM data bus.
AR[8 ... 0]	O	DRAM row/column address.
$\overline{\text{WE}}$	O	DRAM write enable. Active LOW.
$\overline{\text{CAS0}}$	O	Column address select signal (lower data byte).
$\overline{\text{CAS1}}$	O	Column address select signal (upper data byte).
$\overline{\text{RAS}}$	O	DRAM row address select.

Boundary Scan

Mnemonic	Type	Name and Function
TDI	I	Test Data Input, test data sampled at rising edge of TCK.
TDO	O	Test Data Output.
TCK	I	Test Clock Input.
$\overline{\text{TRST}}$	I	Boundary scan reset.
TMS	I	Test Mode select.

Miscellaneous

Mnemonic	Type	Name and Function
SYSCLK	I	40 MHz system clock.
CLKNFS	I	Audio clock input. Can be either an 11.2896 MHz, 16.9344 MHz, or 33.8688 MHz CD–clock.
$\overline{\text{ROME}}$	I	ROM enable. Active LOW input. When asserted the IMPEG IC has to generate a $\overline{\text{DTACK}}$.
$\overline{\text{PULP}}$	O	General purpose output pin. Can be set to LOW or tri–state via an internal register.
$\overline{\text{RESET}}$	I	Global chip reset. Active LOW.

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HARDWARE STRUCTURE

The MCD270 IMPEG chip contains several major functional areas, as illustrated in Figure 2.

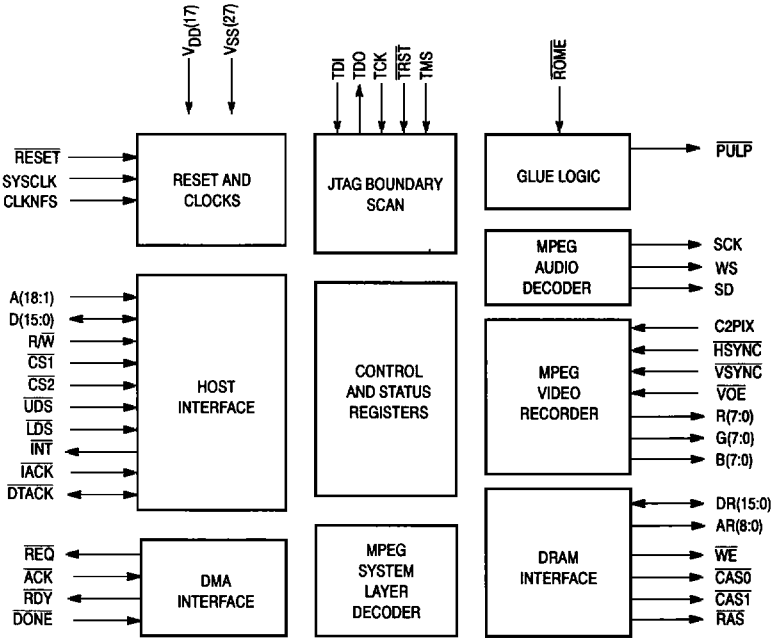

Figure 2. MCD270 Block Diagram

EXTERNAL INTERFACES

Host Interface

The host communicates with the MPEG decoder via the host interface which consists of a 16–bit wide bidirectional data bus, address bus, and necessary signals for interrupt, register access, and DMA.

Four types of data are communicated through the host interface, as follows:

- MPEG video data: Video data being transferred from the host can either be under the control of the CPU (register access) or under control of DMA (burst mode).
- MPEG audio data: Audio data being transferred from the host to the decoder can either be under the control of the CPU (register access) or under control of DMA (burst mode, same channel as video DMA).
- Control and information data: This is bidirectional data transfer. The MCD270 can provide status information to the host via 16–bit wide registers, and the host can control the chip via the registers. The occurrence of some events can be signalled to the host via an interrupt.
- Random access data: The random access feature can only be used when the decoder is in transparency or debug mode. In these modes the complete DRAM can be accessed.

Video Interface

The video interface is the link between the MPEG decoder and the external video DAC.

The video data output can be either in 24–bit RGB or in 24–bit YUV format.This format is selected by bit 6 (RGB) of the Video System Control Register (VSCR).

Audio Interface

The audio interface is in either the Phillips I^2S format or the Sony format. The selection is done with bit 8 of the Global Control Register (GCR).

The MCD270 is always master; it always generates its own wordselect and output sample clock.

DRAM Interface

The DRAM interface consists of the signals necessary to control the external 4 Mbit DRAM.

Boundary Scan

Test and boundary scan signals.

Clock Interface

System and CD clock signals.

Glue Logic

General purpose signals which may be used in a CD–i full motion video cartridge application.

INTERNAL FUNCTIONALITY

The MCD270 consists of audio, video, and general registers. The logical data flow between the main elements in the chip are illustrated in Figure 3.

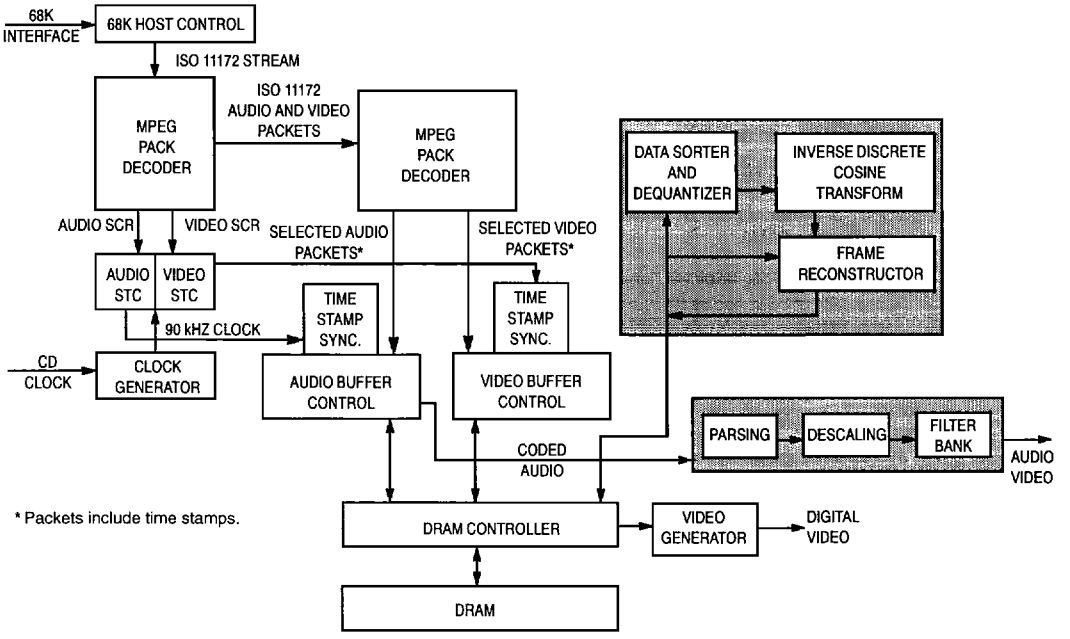

Figure 3. MCD270 Logical Data Flow and Synchronization Diagram

REGISTER MEMORY MAPS

VIDEO REGISTERS

The video registers handle the picture attributes (color, picture height and width, pixel aspect ratios) plus timing and control functions.

Table 1. Temporal Buffer Registers

Address (HEX)	Register	Description
2	T_PWI	Temporal picture width
4	T_PHE	Temporal picture height
6	T_PRPA	Temporal picture rate/aspect ratio

Table 2. Display Control Buffer_0 Registers

Address (HEX)	Register	Description
1C	B0_TCH	Disp_ctrl_buf_0 time_code_high
1E	B0_TCL	Disp_ctrl_buf_0 time_code_low
20	B0_VSR	Disp_ctrl_buf_0 video status
22	B0_BX	Disp_ctrl_buf_0 first pix of line

Table 3. Display Control Buffer_1 Registers

Address (HEX)	Register	Description
30	B1_TCH	Disp_ctrl_buf_1 time_code_high
32	B1_TCL	Disp_ctrl_buf_1 time_code_low
34	B1_VSR	Disp_ctrl_buf_1 video status
36	B1_BX	Disp_ctrl_buf_1 first pix of line

Table 4. Display Control Buffer_2 Registers

Address (HEX)	Register	Description
44	B2_TCH	Disp_ctrl_buf_2 time_code_high
46	B2_TCL	Disp_ctrl_buf_2 time_code_low
48	B2_VSR	Disp_ctrl_buf_2 video status
4A	B2_BX	Disp_ctrl_buf_2 first pix of line

Table 5. Video Control Registers

Address (HEX)	Register	Description
66	Br	Border_red register
68	Bg	Border_green register
6A	Bb	Border_blue register
6C	Yo	Y–offset register
6E	Xo	X–offset register
70	Ya	Y–active register
72	Xa	X–active register
74	Yd	Y–display register
76	Xd	X–display register
78	Wh	Window height register
7A	Ww	Window width register
7C	Yw	Y–window register
7E	Xw	X–window register

Table 6. Video System Control Registers

Address (HEX)	Register	Description
50	VSTAT	Video decoder status
52	PWI	Picture width
54	PHE	Picture height
56	PRPA	Picture rate/pixel aspect ratio
58	TCH	Time code high
5A	TCL	Time code low
5C	VSR	Video status
5E	VSTS	Video system status
60	VIER	Video interrupt enable
62	VISR	Video interrupt status
64	VTIM	Video timer
C0	VSCMD	Video system command
C2	VCMD	Video command
C4	VSEL	Video stream select
C6	VSCR	Video system control
DE	VDI	Video data input
E4	ABS	Actual buffer size
F2	BSIZ	Block size

Table 7. MMU Registers

Address (HEX)	Register	Description
F4	VFSTART	Video FIFO start point
114	AFSTART	Audio FIFO start point

AUDIO REGISTERS

The audio registers handle the selection and decoding of the audio stream, attenuation, audio frame header updating plus associated timing and interrupts.

Table 8. Audio System Control Registers

Address (HEX)	Register	Description
200	ADCR	Audio decoder command
202	ADSR	Audio decoder status
204	ATIM	Audio timer
106	ABSZ	Audio blocksize
208	ASELS	Select audio stream
20A	ACURS	Current audio stream
11E	ADI	Audio data input
218	ADDLY	Audio decoder delay
21A	AIOR	Audio interrupt originator
21C	AIER	Audio interrupt enable

Table 9. Audio Control and Information Control Registers

Address (HEX)	Register	Description
214	AHR1	Audio header 1
216	AHR2	Audio header 2
20C	ATTL	Attenuator left
20E	ATTR	Attenuator right

GENERAL REGISTERS

Included here are general control registers, interrupt registers, and audio/video sync registers.

Table 10. General Control and Information Registers

Address (HEX)	Register	Description
DA	GCR	Global control register
DC	ICR	Interrupt control
206	SCC	System clock counter
210	AVRH	A/VSYNC high
212	AVRL	A/VSYNC low

DOWNLOAD REGISTERS

The audio and video microcode has to be downloaded from the host.

Table 11. Video Microcode Registers

Address (HEX)	Description
800	Bank1
1000	Bank2
1800	Bank3

Table 12. Audio Microcode Registers

Address (HEX)	Description
2000	Bank1
2800	Bank2
3000	Bank3

ELECTRICAL SPECIFICATIONS

OPERATING RANGE

The limits for operating the device are as follows:

Ambient Temperature (T_A) ..... 0 – 70°C
Voltage, V_{DD} ..... 5 V ± 10%
Voltage, V_{SS} ..... 0 V

ABSOLUTE MAXIMUM RATINGS* (Voltages Referenced to V_{SS}, Unless Otherwise Noted)

Symbol	Parameter	Min	Max	Unit
V_{DD}	Supply Voltage	– 0.5	+ 7.0	V
V_I	Input Voltage	– 1.5	V_{DD} + 1.5	V
V_O	Output Voltage	– 0.5	V_{DD} + 0.5	V
I_O	Output Current	—	± 25	mA
P_d	Power Dissipation	—	1200	mW
T_{stg}	Storage Temperature	– 65	+ 150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit.

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DC ELECTRICAL CHARACTERISTICS (V_{DD} = 5 V ± 10%, V_{SS} = 0 V, T_A = 0 to + 70°C, Unless Otherwise Noted)

Parameter	Symbol	Conditions	Min	Max	Unit
Operating Supply Current	I_{DD}	40 MHz	—	300	mA
Input Voltage (TTL Input)	V_{IH} V_{IL}		2.0 —	— 0.8	V
Output Voltage, 8 mA	V_{OH} V_{OL}		3.5 —	— 0.4	V
Output Voltage, 16 mA	V_{OH} V_{OL}		3.5 —	— 0.4	V
Power Dissipation			—	1500	mW

NOTE: All outputs can have a load of 130 pF, except for the DRAM which can have 50 pF.

IMPEG/CD–i ARCHITECTURE

In a CD–i player as shown in Figure 4, IMPEG provides the complete functionality of full motion extensions as specified in the Green Book standard for CD–i. It requires the external 4 Mbit DRAM to support MPEG video and MPEG audio decoding, but can use the video and audio DACs already part of the base case CD–i architecture. IMPEG audio decoding is synchronized to the CD drive clock and its audio output is added to base case audio. IMPEG video decoding is synchronized to the base case video decoder (MCD211, VDSC), and its video output is multiplexed with VDSC output on a pixel by pixel basis.

Digital Video Switching Between VDSC and IMPEG

Digital or analog multiplexing may be used with IMPEG. Figure 5 shows how only one video and one audio DAC may be used if digital multiplexing is used. Digital audio is sent directly to the base case audio decoder (MCD221 CIAP) and is digitally mixed before a combined signal is sent to the audio DAC. Digital video is tied directly to the 24–bit RGB bus from the base case video decoder (MCD211 VDSC) and multiplexing is achieved by a switch signal from VDSC, which enables and disables pixel outputs from the two sources.

Analog Video Switching Between VDSC and IMPEG

Figure 6 shows a configuration more suited to a cartridge based approach in which MPEG1 is added to a basic CD–i player as an expansion cartridge. IMPEG audio and video decoding are still synchronized to the relevant base case signals, but the multiplexing and mixing are done in the analog domain. Although this requires two DACs, it requires fewer pins on the expansion cartridge connector.

IMPEG IN A PC MULTIMEDIA APPLICATION

Figure 7 illustrates how IMPEG could be used in a PC based application to provide an MPEG playback window overlayed on a VGA display. The VGA overlay controller provides scan rate conversion of the decoded MPEG image and windowing control based on color keying or programmable XY coordinates. An analog video switch is controlled from this to provide the overlay function.

Using IMPEG in this standalone manner requires the addition of a TV sync generator to provide $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, and a pixel clock to IMPEG.

VIDEO ON DEMAND

IMPEG may be used as the decoder section of a video on demand integrated receiver decoder, as illustrated in Figure 8. MPEG1 video and audio streams are carried over an asymmetric digital subscriber loop (ADSL) in an MPEG2 transport stream. A transport stream decoder separates the conditional access data and the video and audio streams from the transport stream. The video and audio streams are directed to IMPEG and the conditional access data to the Smart Card controller. An on–screen display is generated by using an MCD211 (VDSC). The video and audio output stages are identical to those in the CD–i application described earlier.

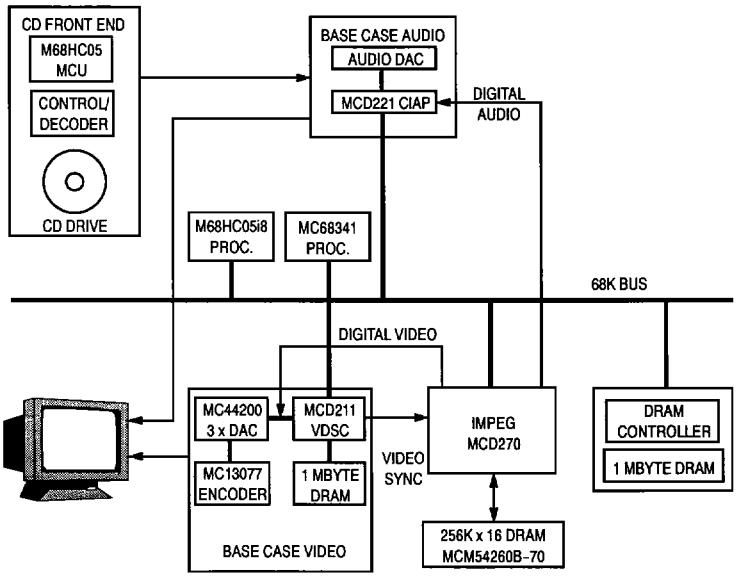

Figure 4. IMPEG/CD–i Architecture

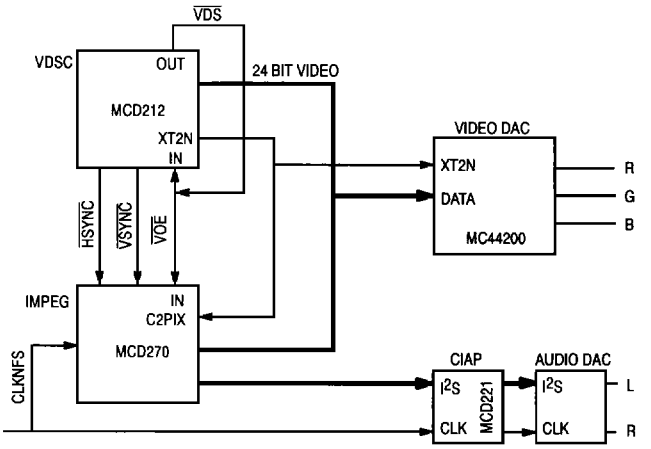

Figure 5. Digital Video Switching Example

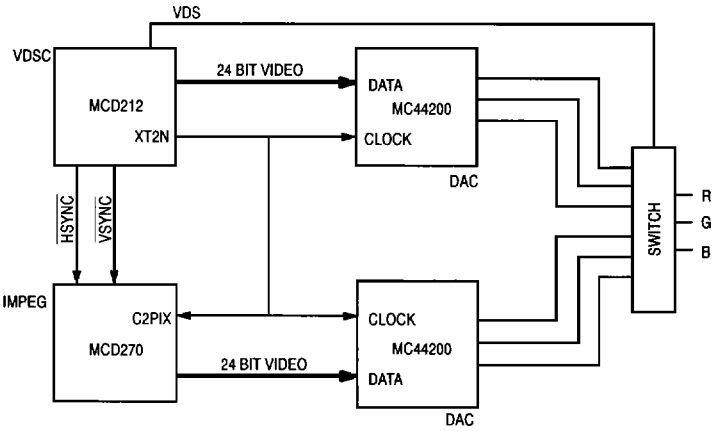

Figure 6. Analog Video Switching Example

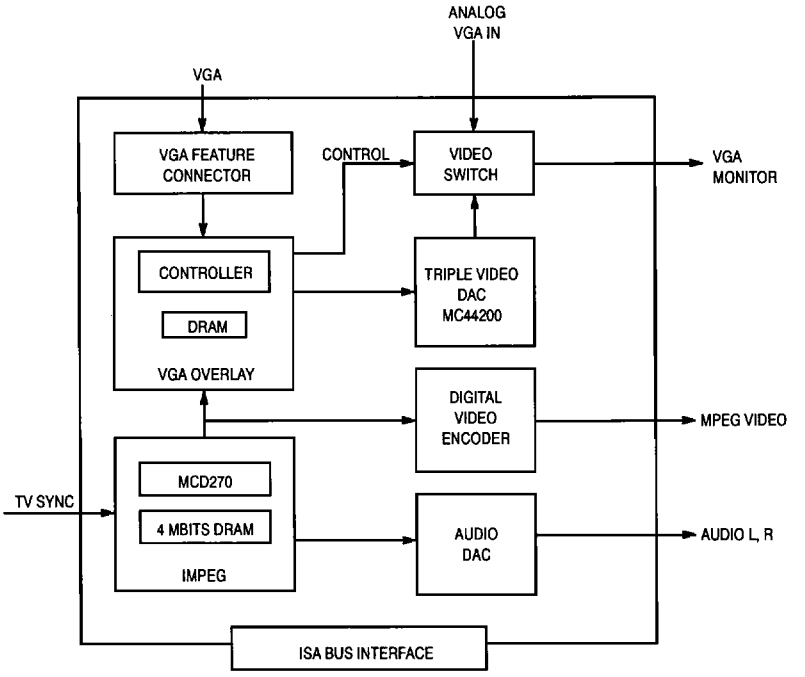

Figure 7. Example of IMPEG in a PC Multimedia Application

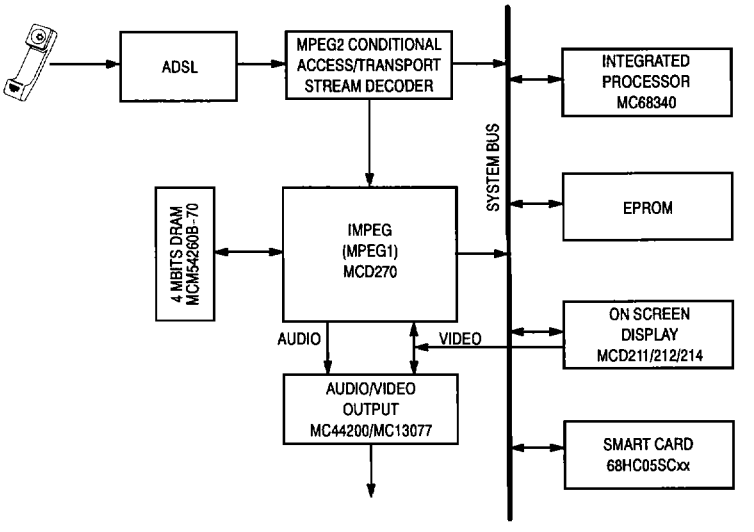

Figure 8. Video On Demand Example