

Service
Service
Service

Interactive
Media
Systems

CD-I



CDI 205

Service Manual

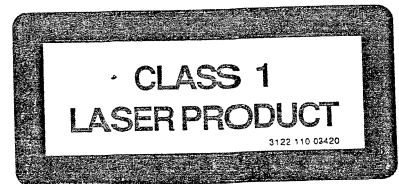


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- 1 Manual information
- 2 Product information
- 3 Service information
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- 7 Diagnostics, measurements and adjustments

Safety regulations require that the set be restored to its original condition and that parts which are identical with those specified be used.

Pour votre sécurité, ces documents doivent être utilisés par des spécialistes agréés, seuls habilités à réparer votre appareil en panne.



PHILIPS

- * AM noise : output of measured value in dB referred to the average amplitude of the colour subcarrier burst applied
- ** PM noise : output of measured value in dB referred to the constant phase of a reference oscillator

Y/C (S-Video) output:

Type of connector : Mini-Din 4 (female)
 Pinning:

No.	Function
1.	Gnd Y
2.	Gnd C
3.	Y
4.	C

PAL amplitude : $Y = 1V_{pp} + 15\% / -10\%$
 into 75 Ohm
 amplitude : $C = 300 mV_{pp} + / - 10\%$ (burst)
 bandwidth Y : = 5 MHz (-3dB)
 bandwidth C : = 1.6 MHz
 S/N on Y output (10KHz-5MHz) : > 48 dB
 (10KHz-10MHz) : > 45 dB
 S/N on C output : AM (*) > 55 dB
 PM (**) > 50 dB

- * AM noise : output of measured value in dB referred to the average amplitude of the colour subcarrier burst applied
- ** PM noise : output of measured value in dB referred to the constant phase of a reference oscillator

Laser Detector Grating Unit (LDGU)

Laser type : semi conductor AlGaAs
 Wave length : 780 nm
 Output power : 3.3 mW typical

RS232-1 (port 1) communication:

Connector type : 8 pins miniDIN (female)
 Location : front
 Internal device : MMC slave proc. (68HC05, SCI+ports)
 Baudrates : 1200 and 9600
 Dataformat : 1 startbit
 7 databits
 2 stopbits
 no parity
 Handshake : hardware: only RTS
 software: not available

Signals & Pinning:

pin	signal	description	Inp/Outp
1	n.c.	Not Connected	
2	RXD	Received Data	Input
3	TXD	Transmitted Data	Output
4	DTR (*)	Data Terminal Ready	Output
5	GND	Signal Ground	
6	n.c.	Not Connected	
7	RTS	Request To Send	Output
8	+5V	Power supply for the device	

RS232-2 (port 2) communication:

Connector type : 8 pins miniDIN (female)
 Location : rear
 Internal device : on chip UART (SCC68070)
 Baudrates : 75, 150, 300, 1200, 2400, 4800, 9600 and 19200
 Dataformat : character length: 7 or 8 bits
 stopbit length : 1 or 2 bits
 parity : odd, even or no
 Handshake : hardware: 2 control lines; RTS and CTS.
 software : XON/XOFF.

Signals & Pinning:

pin	signal	description	Inp/Outp
1	n.c.	Not Connected	
2	RXD	Received Data	Input
3	TXD	Transmitted Data	Output
4	DTR (*)	Data Terminal Ready	Output
5	GND	Signal Ground	
6	CTS	Clear To send	Input
7	RTS	Request To Send	Output
8	+5V	Power supply for the device	

Input : this is an input signal for the CD-I player
 Output: this is an output signal for the CD-I player.

(*) DTR is not an active handshake signal. It serves as a power supply for some input devices.

All signal levels and current ratings, except +5V and DTR are according EIA RS-232-C standard.

RATINGS : +5V +/-10% max. 200mA
 DTR : +12V +/-10% max. 10mA (Ri = 1kΩ)

IR interface:

The IR (infra red) receiver for use with the CD-I remote control.
 Specification according UAW-0422

characteristics
 Data format : RC-5 extended format
 infrared transmission data.
 Distance : 20 - 800 cm.
 Sampling time : =< 50 ms
 Receive angle : 45 degree out of the centre line

Infrared receiver control Device : GP1U501X SHARP

Mains socket:

Connector : 2-pol.

The player has to be Class I equipment.

Modifications without notice

2 PRODUCT INFORMATION

2.1 TECHNICAL SPECIFICATION

Physical

Dimensions (w x h x d)
420 x 90 x 400 mm
(16.5 x 3.5 x 15.7 inch)

Weight (approx.)
7 kg
(15.4 lbs)

Power supply

220/240 V ; 50-60Hz
220V range 198V to 264V

Power consumption

Approx. 35W

Approvals

FCC, UL
Conforms with VDE, FTZ, CSA, Nordic, US and GERMAN
laser safety regulations

Audio L+R:

Connector
Type Cinch connector gold plated 2x
Colour Left : white
Right:red

Output quality in case of CD-DA

Measurements acc. to IEC TC 60 Subcan. 60A
Output level : 2Vrms +/- 3 dB
Frequency range : 20 Hz to 20 kHz
Frequency linearity : +0.2 dB/ -0.2 dB
Cross talk (1kHz) : - 86 dB
Harmonic dist.
+ noise at 1kHz : - 86 dB
S/N ratio : 87 dB (typ >90)
Dynamic range : 86 dB

Output quality in case of ADPCM to be specified

Headphone output:

Connector type : Phone socket
Output control : Manual volume control

Output quality in case of CD-DA

Load impedance range : 8 Ohm - 2 kOhm
Output power : 30 mW at 1kHz, 32 Ohm
Frequency range : 20 Hz - 20 kHz +/- 3 dB
Harmonic distortion (1kHz) : - 83 dB
S/N ratio : 84 dB
Dynamic range : 83 dB
Cross talk $R_i=600E$ (1kHz) : - 75 dB

Video specifications

625 lines: RGB (PAL, SECAM) for /00/05

Connector type : Euroconnector (SCART)
Pinning:

No.	Function
1.	Audio R (analogue)
2.	NC
3.	Audio L (analogue)
4.	Audio ground
5.	Blue ground
6.	NC
7.	Blue
8.	Slow switching(0=TV, 1=Euroconn.)
9.	Green ground
10.	NC
11.	Green
12.	NC
13.	Red ground
14.	NC
15.	Red
16.	Fast switching (RGB/CVBS)
17.	CVBS ground
18.	Fast switching ground
19.	CVBS/RGB sync
20.	NC
21.	Shield

Video interface

General information:

TABEL 1 Encoded RGB

General information : PAL Environment
Resolution normal H*V : 384*280
384*560
Line period : 64.00 us
Active line period : 51.20 us
VSC clock : 30.0000 MHz

Display format
non-interlace : 312 lines
interlace : 625 lines
(2 different frames)
interleaved : 625 lines
(2 identical frames)

PAL
Amplitude : 700mVpp +/- 10%
(max. white level)
Line time : 64. uS
Sync. output : 300 mVpp +/- 0.1V
into 75 Ohm
S/N on RGB output : > 50 dB (40 Hz - 5 MHz)
S/N on RGB output : > 45 dB (40 Hz - 10 MHz)
Bandwidth on RGB out : - 3 dB at 7.5 MHz

CVBS output:

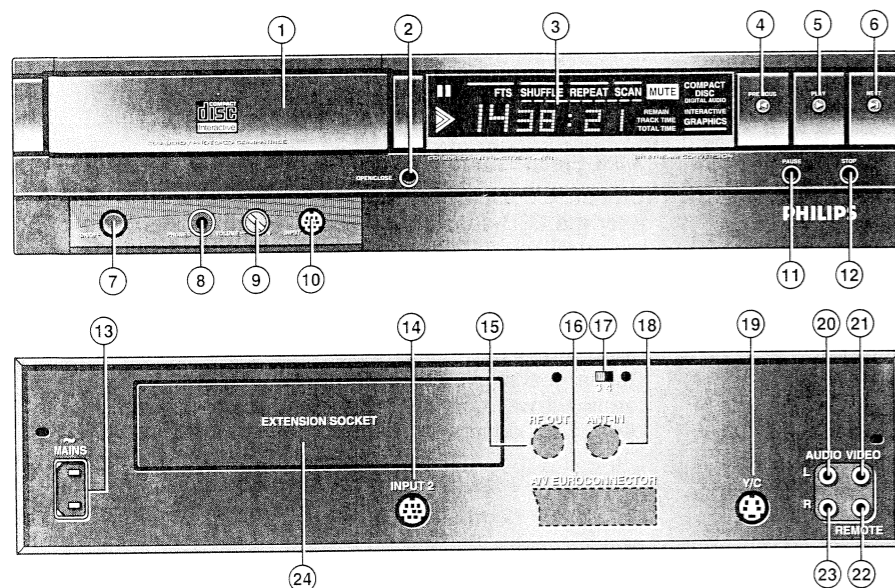
Connector : Cinch connector,
colour Yellow

PAL
Amplitude : 1Vpp +15%/-10%
White bar : 700 mVpp +110 mV/-70 mV
Sync amplitude : 300 mVpp +/-40 mV
Burst amplitude : 300 mV +/-30 mV
S/N lum. (40Hz-10MHz) : fsc notch >45dB
S/N chrom. in red : AM (*) > 48 dB
PM (**) > 43 dB
Video bandwidth : 4.5 MHz (-6dB)
Chroma subc. freq. : = 4.433661 MHz
X-tal locked +/-50Hz

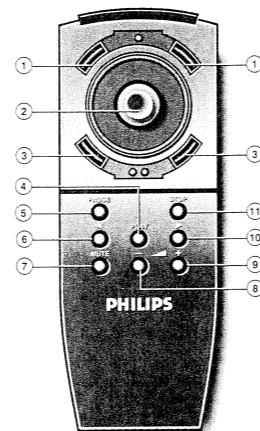
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2.2 CONNECTIONS AND CONTROLS



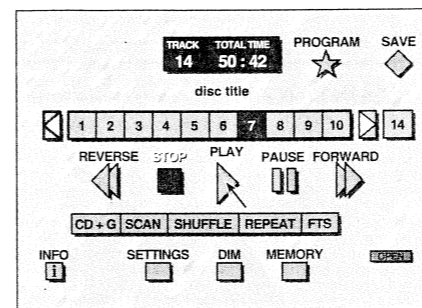
Front panel control functions and rear connections



22ER9051 Infra red remote control

The user shell

With just the one "point and click" operation, player functions can be controlled so easily that the actions become intuitive. This is because of the player's specially designed "user shell" program, which presents a series of screen displays that not only allow you a complete choice of play functions, but also guide you in selecting them.



User shell screen

When the player is switched on, the first "user shell" screen invites you to load a disc. Playing a CD-I disc is a simple matter of loading the disc and selecting "Start" on the "CD-I start" screen which then automatically appears. The CD-I program starts to run, and you select options from the screen according to choice.

For CD-Digital Audio discs, the "user shell" presents a play control screen. This offers more than just the functions fitted as standard on CD players (and also provided on the front panel and remote control). It offers all the features found only on top-of-the-range players. These include Program, Favorite Track Selection, Title, Shuffle, Repeat, Play and Scan:

Another "user shell" screen offers "Personal Preference" settings. These include date and time display, Scan time, Auto Shuffle, and Repeat. When "Personal Preference" settings have been made, the player automatically adopts them when starting up.

Further "user shell" screens provide information, CD-DA programming (FTS) facilities, a list of stored programs and other information, and control for CD Graphics.

User Shell Functions

General screens:

- "Personal Preference" settings screen: Auto Shuffle, Auto FTS, Display Time/Date, Scan Time, Repeat (Disc or Track).
- Open/Close (on player start-up screen).
- Info screens (depending on version with language choice).
- Memory screen (manages CD-I stored data, as well as FTS programs and titles).
- Dim Screen (adjusts screen brightness).

CD-I start-up screen:

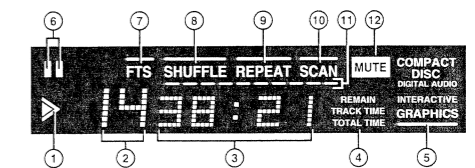
- Start CD-I (starts CD-I or Photo-CD application).

CD-Digital Audio screen:

- While Playing: Play, Stop and Pause.
- Play Modes: Scan, Shuffle, Repeat and FTS.
- Control: Fast Forward, Fast Rewind, Next Track (directly selectable), Previous Track (directly selectable), Program (programming of selected tracks in any order), Save (stores your favorite track programme and allows manual input of titles related to discs or FTS programs).

Soft-tone fluorescent tube display (FTD)

The multifunction FTD supplies complete and continuously up-dated information on the player status.



- 1 Disc playing
- 2 Track or fragment
- 3 Minutes and seconds.
- 4 Time indicators: show that the time displayed is Track Time, Total Time, Remaining Track Time, or Remain.
- 5 Type of disc: Compact Disc Interactive, Compact Disc Digital Audio, Compact Disc Digital Audio with Graphics
- 6 Pause active
- 7 FTS active
- 8 Shuffle active
- 9 Repeat active
- 10 Scan active
- 11 Scan timing strip (lights progressively during each scan period)
- 12 Mute*

*depending on version

CDI front panel controls

1. Disc loading tray with "touch to close" action
2. Open/close key
3. Soft tone multifunction display with infra-red remote control receiver
4. "Previous" key for instant track skip
5. "Play" key
6. "Next" key for instant track skip
7. Power "On/Off" key
8. Headphone socket
9. Headphone volume control
10. I/O port for CD-I pointing devices
11. Pause key
12. Stop key

CDI rear panel connections

13. Power input socket
14. I/O port for CD-I pointing devices, keyboard or other RS232 connection
15. Antenna out*
16. Euroconnector*
17. Channel selector*
18. Antenna in*
19. Y/C (S-video) output
20. Audio output L
21. CVBS (video) output
22. Remote control in
23. Audio output R
24. Extension socket (for 22ER9141 Digital Audio/Video module)

*depending on version

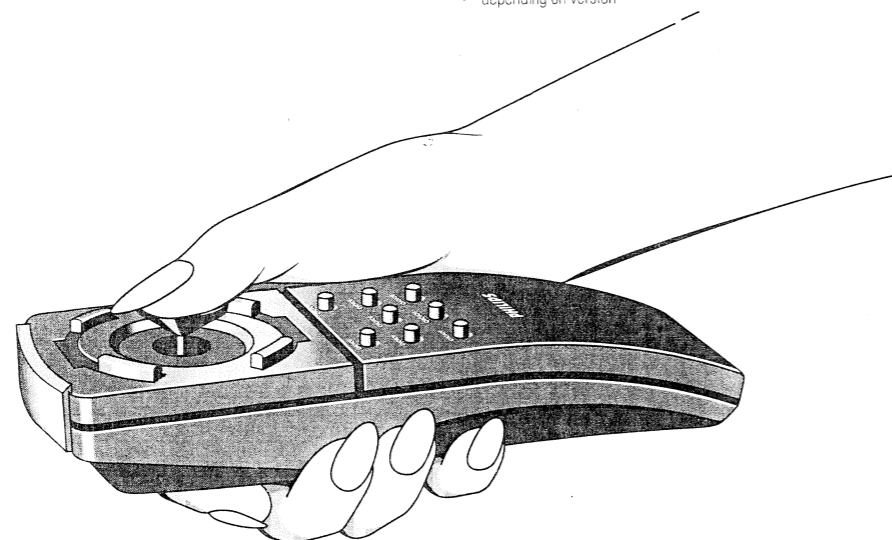
The "Thumbstick" remote control

The shape and layout of the "Thumbstick" control were the subject of careful ergonomic studies to ensure that it can be used left-handed or right-handed, in big or small hands.

- 1/3 Action keys
- 2 Thumbstick
- 4 "Play" key
- 5 "Pause" key
- 6 "Previous" key for instant track skip
- 7 Mute or TV/CDI selector key*
- 8 Volume control down key
- 9 Volume control up key
- 10 "Next" key for instant track skip
- 11 "Stop" key

*depending on version

The control sits conveniently in the hand, and the thumbstick and action keys, which are by far the most-used controls, are easily operated one-handed.



Input P



- | Pin | Signal |
|-----|--------|
| 1 | NC |
| 2 | R |
| 3 | TX |
| 4 | D1 |
| 5 | Gf |
| 6 | C1 |
| 7 | R1 |
| 8 | +E |

A/V Co

- CVBS or (cinch):
Audio o (2 x cinch)
Remote (cinch):
Antenn:
RF outp
Headph (6.3 mm)

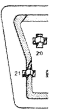
Y/C (S-



- | Pin | Signal |
|-----|--------|
| 1 | Gf |
| 2 | Gf |
| 3 | Y |
| 4 | C |

Eurocc

- | Pin | Signal |
|-----|--------|
| 1 | A |
| 2 | N |

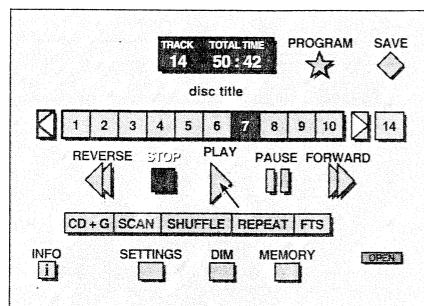


- | Pin | Signal |
|-----|--------|
| 3 | A |
| 4 | A |
| 5 | B |
| 6 | N |
| 7 | B |
| 8 | S |
| 9 | G |
| 10 | N |
| 11 | G |
| 12 | N |
| 13 | R |
| 14 | N |
| 15 | R |
| 16 | F |
| 17 | C |
| 18 | F |
| 19 | C |
| 20 | N |
| 21 | S |

*depend

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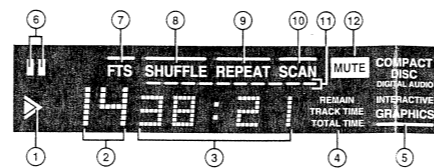
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- 10 Scan active
- 11 Scan timing strip (lights progressively during each scan period)
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*depending on version

Input Port

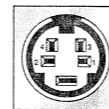


Pin	Signal	Function	I/O
1	NC	Not connected	
2	RXD	Received Data	I
3	TXD	Transmitted Data	O
4	DTR	Data Terminal Ready	O
5	GND	Signal Ground	
6	CTS	Clear to Send	I
7	RTS	Request to Send	O
8	+5V	Power supply to device	

A/V Connections

CVBS output (cinch):	1 Vpp into 75 Ohm
Audio output (2 x cinch):	2 Vrms into 75 Ohm
Remote in (cinch):	2 Vpp at 2.2 kOhm
Antenna input:	75 Ohm*
RF output:	75 Ohm*
Headphone (6.3 mm socket):	8 Ohm - 2 kOhm

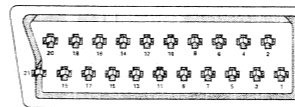
Y/C (S-Video) Connector



Pin	Function
1	Ground Y
2	Ground C
3	Y
4	C

Euroconnector*


Pin	Function
1	Audio R (analogue)
2	NC



3	Audio L (analogue)
4	Audio ground
5	Blue ground
6	NC
7	Blue
8	Slow switching (0 = TV, 1 = Euroconnector)
9	Green ground
10	NC
11	Green
12	NC
13	Red ground
14	NC
15	Red
16	Fast switching (RGB/CVBS)
17	CVBS ground
18	Fast switching ground
19	CVBS/RGB sync
20	NC
21	Shield

*depending on version

3.1 SAFETY INSTRUCTIONS

– Safety regulations demand that the set be restored to its original condition and that components identical with the original types be used.
Safety components are marked by the symbol .

– ESD

All IC's and many other semi-conductors are susceptible to electrostatic discharges (ESD). Careless handling during repair can reduce life drastically.
When repairing, make sure that you are connected with the same potential as the mass of the set via a wrist wrap with resistance.
Keep components and tools also at this potential. For detailed information see "Handling ESD-sensitive components".

– A set to be repaired should always be connected to the mains via a suitable isolating transformer.

– never replace any modules or any other parts while the set is switched on.

– Use plastic instead of metal alignment tools. This in order to preclude short-circuit or to prevent a specific circuit form being rendered unstable.

3.2 SERVICING OF SMDs (Surface Mounted Devices)

3.2.1 General cautions on handling and storage

- Oxidation on the SMDs terminals results in poor soldering. Do not handle SMDs with bare hand.
- Avoid for storage places that are sensitive to oxidation such as places with sulfur or chlorine gas, direct sunlight, high temperatures or a high degree of humidity.
As a result the capacitance or resistance value of the SMDs may be affected.
- Rough handling of circuit boards containing SMDs may cause damage to the components as well as the circuit boards. Circuit boards containing SMDs should never be bent or flexed. Different circuit board materials expand and contract at different rates when heated or cooled and the components and/or solder connections may be damaged due to the stress. Never rub or scrape chip components as this may cause the value of the component to change. Similarly, do not slide the circuit board across any surface.

3.2.2 Removal of SMDs

- Heat the solder (for 2-3 seconds) at each terminal of the chip. Small components can, by means of litz wire and a limited horizontal force, be removed with the soldering iron. They can also be removed with a solder sucker (see Fig. 1a) or
- While holding the SMD with a pair of tweezers take it off gently using the soldering iron's heat applied to each terminal (see Fig. 1b).
- Remove the excess solder on the solder lands by means of litz wire or a solder sucker (see Fig. 1c).

3.2.2.1 Caution on removal:

- When handling the soldering iron, use suitable pressure and be careful.
- When removing the chip, do not use undue force with the pair of tweezers.
- The soldering iron to be used (approx. 30 W), must preferably be provided with a thermal control (soldering temperature about 225 to 250°C).
- The chip, once removed, must **never** be used again.

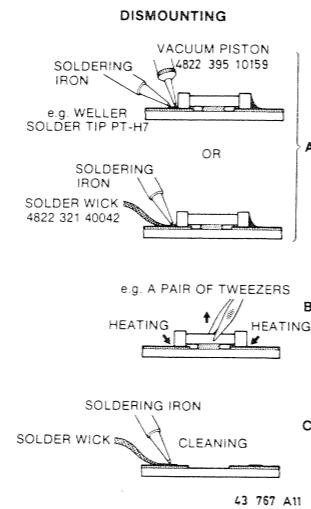


Fig. 1

3.2.3 Attachment of SMDs

- Locate the SMD on the solder lands by means of tweezers and solder the component at one side. Ensure that the component is positioned well on the solder lands (see Fig. 2a).
- Next complete the soldering of the terminals of the component (see Fig. 2b).

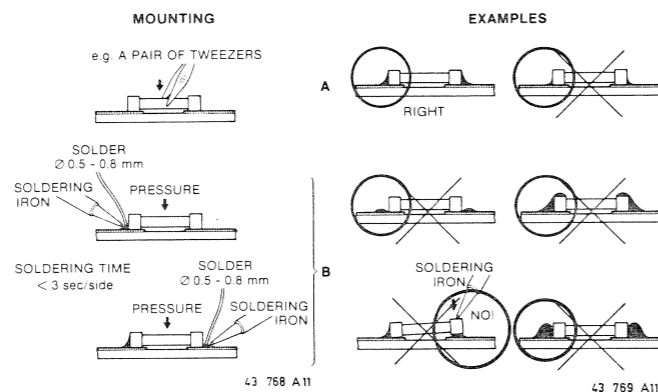
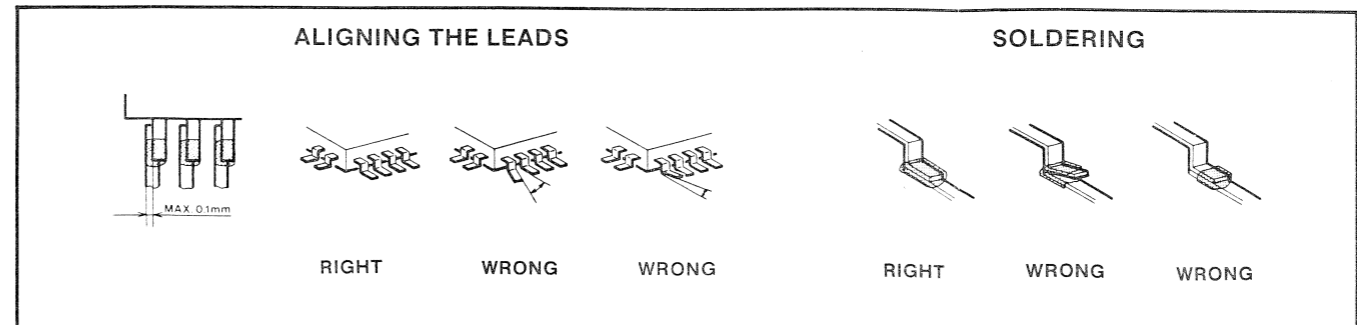
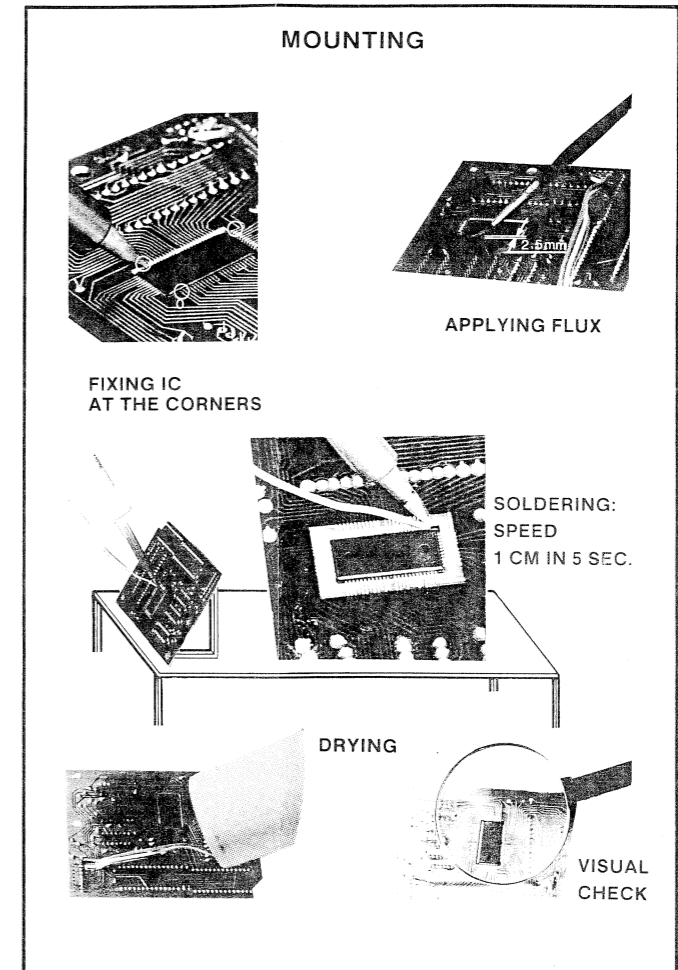
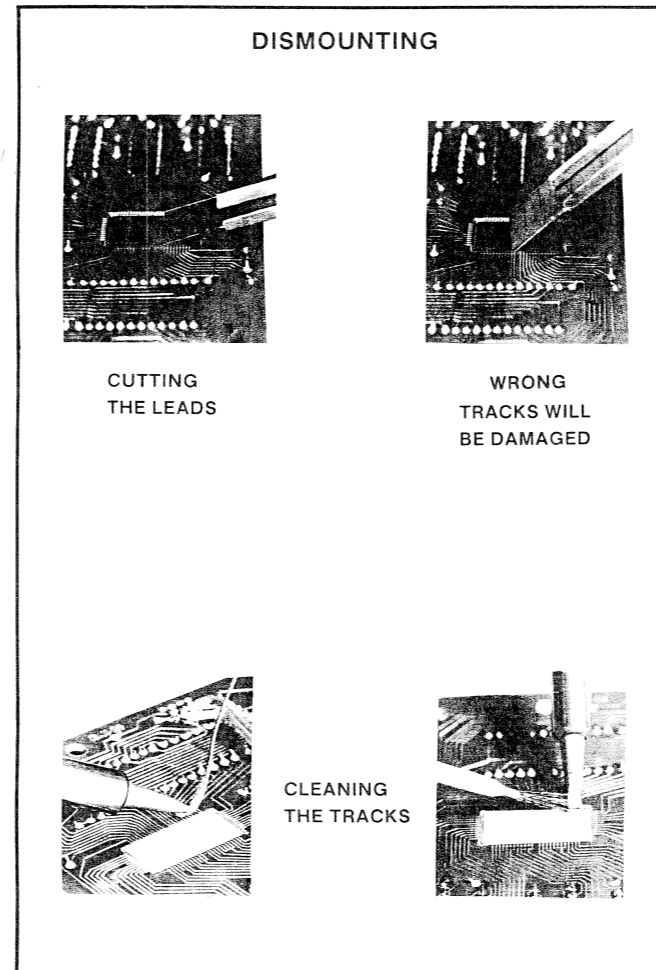
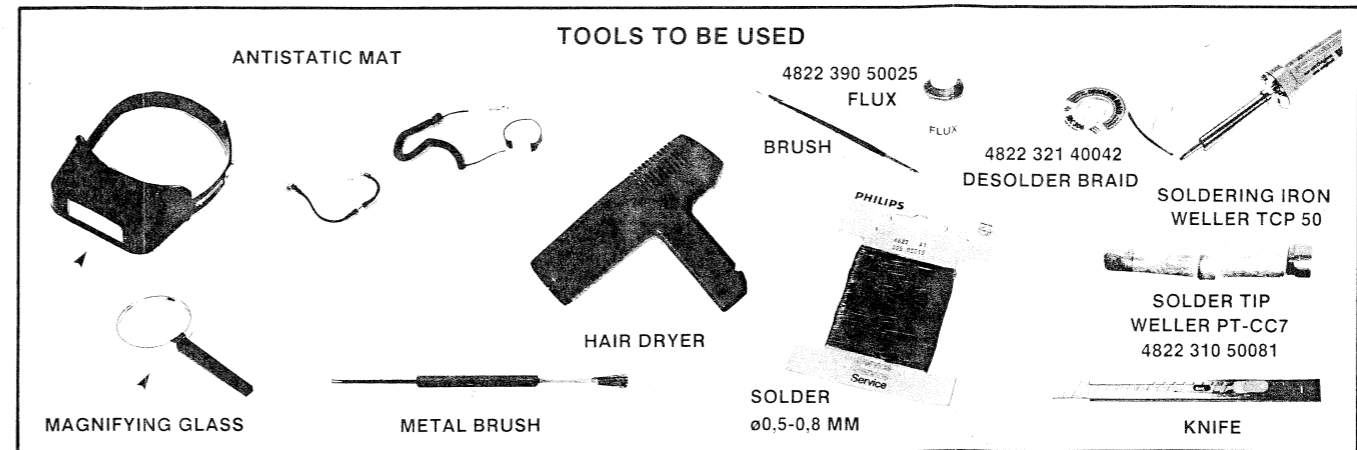


Fig. 2

Fig. 3

3.2.3.1 Caution on attachment:

- When soldering the SMD terminals, do not touch them directly with the soldering iron. The soldering must be as quick as possible; care must be taken to avoid damage to the terminals and the body itself.
- Keep the SMD's body in contact with the printed board when soldering.
- The soldering iron to be used (approx. 30 W) must preferably be provided with a thermal control (soldering temperature about 225 to 250°C).
- Soldering should not be done outside the solder land.
- Soldering flux (of rosin) may be used but should not be acidic.
- After soldering, let the SMD cool down gradually at room temperature.
- The quantity of solder must be proportional with the size of the solder land. If the quantity is too great, the SMD might crack or the solder lands might be torn loose from the printed board (see Fig. 3).



3.3 HANDLING ESD-

3.3.1 Personal safety

The testing, handling components requires safety. A person deal components should, via a resistance to the of the set to protect the supply voltage. This resistance is of wrist wraps. If nec transformer.

3.3.2 Storage and tra

Transport and store i original packages. As an alternative to t a conductive material short-circuits all the p another. Always discharge the

3.3.3 Testing or hanc

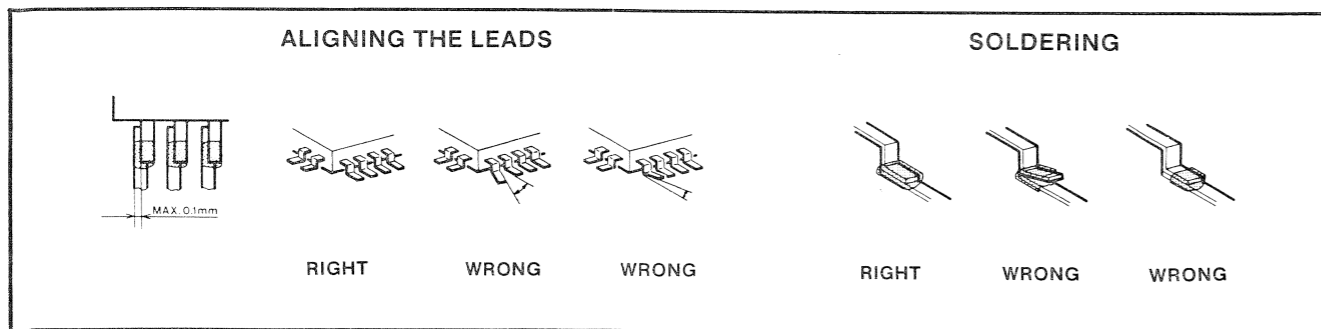
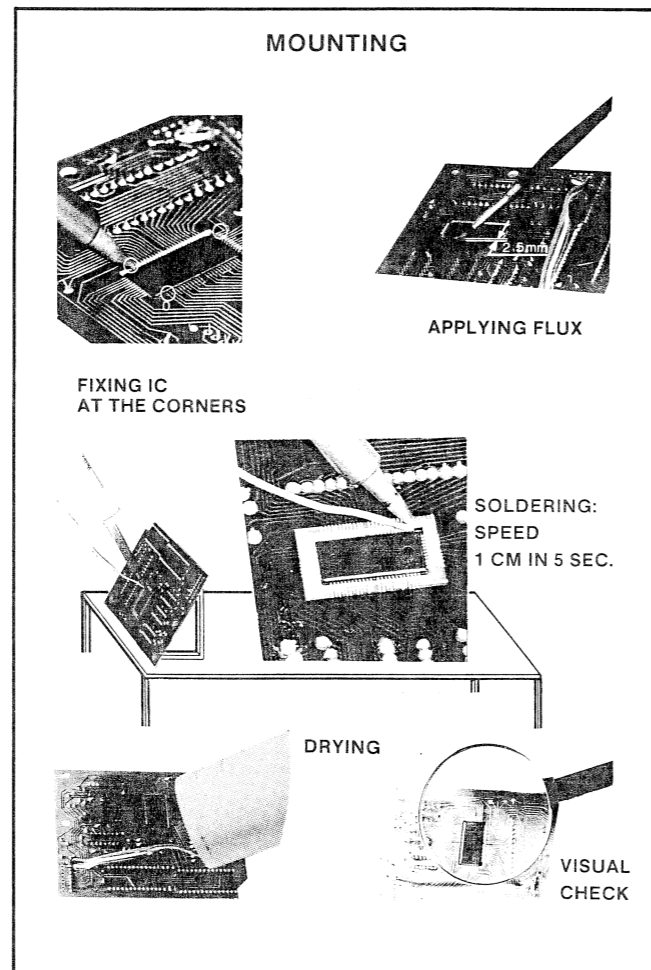
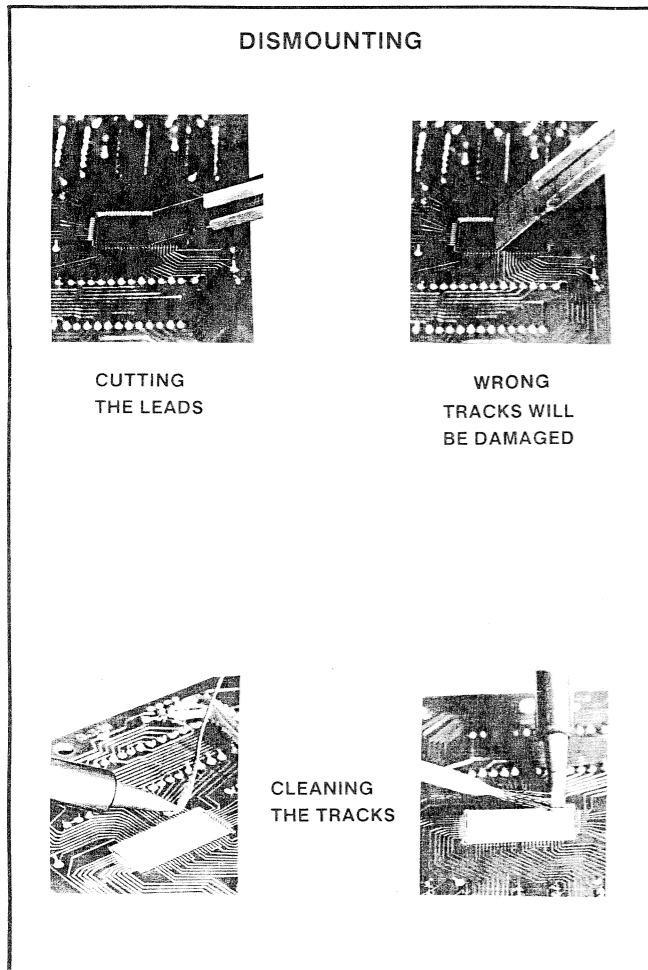
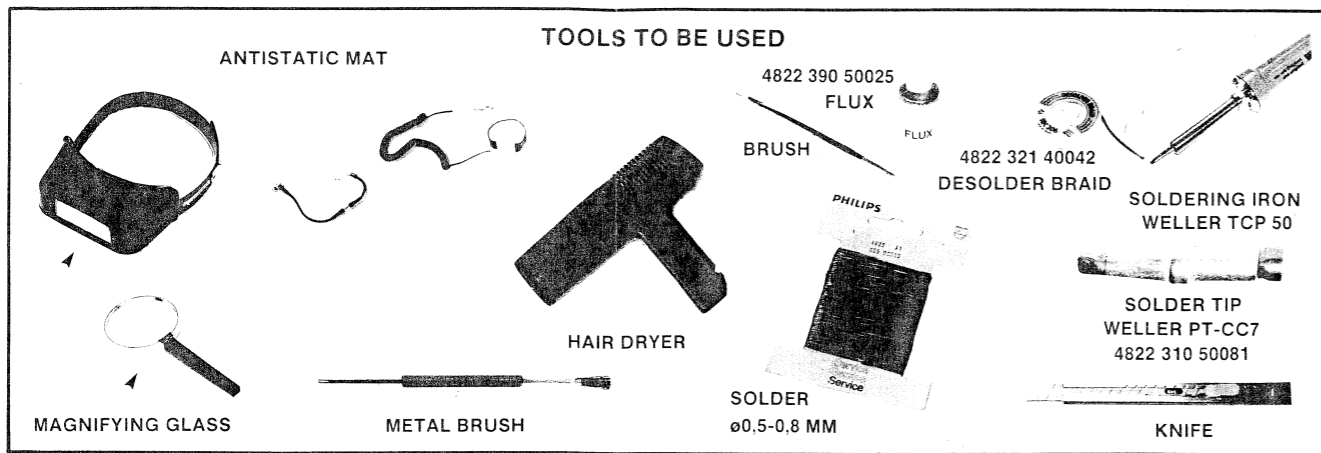
Work on a conductive circuits and compone components and circ another. Use a conductive wri electrical connection and yourself via a res the wrist wrap. Connect equipment a surface. Do not connect any s power supply of the : All the inputs that are either to ground or to testing, do not use ar of sensitive compone

3.3.4 Mounting ESD-

Mount ESD-sensitive components have be Make sure that the o parts of the PCB, mc operator are at the s of the set. If it is imposssible to c operator should pick into contact with the

Condu

Special attention shou dry atmosphere and w nylon carpet or such.



3.3 HANDLING ESD-SENSITIVE COMPONENTS

3.3.1 Personal safety

The testing, handling and replacing of ESD-sensitive components requires special attention for personal safety. A person dealing with ESD-sensitive components should, normally speaking, be connected via a resistance to the same potential as the chassis of the set to protect him against direct contact with the supply voltage. This resistance is often applied in the connection lead of wrist wraps. If necessary, make use of an isolating transformer.

3.3.2 Storage and transport

Transport and store the circuits and PCBs in their original packages. As an alternative to the original package one may use a conductive material or special IC package which short-circuits all the pins of the component with one another. Always discharge the package before opening it.

3.3.3 Testing or handling

Work on a conductive surface when testing loose circuits and components or when transferring components and circuits from one package to another. Use a conductive wrist wrap with lead to make an electrical connection between the conductive surface and yourself via a resistance in the connection lead of the wrist wrap. Connect equipment and tools also with this conductive surface.

Do not connect any signals to inputs as long as the power supply of the set to be tested is off. All the inputs that are not used should be connected either to ground or to the supply voltage. When testing, do not use any freon sprays for under-cooling of sensitive components.

3.3.4 Mounting ESD-sensitive components

Mount ESD-sensitive components only after all other components have been mounted. Make sure that the components themselves, the metal parts of the PCB, mounting equipment and mounting operator are at the same potential level as the chassis of the set. If it is impossible to ground the PCB, the mounting operator should pick the PCB up before bringing it into contact with the components to be replaced.

3.3.5 Soldering

Soldering iron tips, also those of low-voltage soldering stations, should be kept at the same potential as the components and the PCB. It is better to use solder-removing braid than solder suckers.

3.3.6 Electrostatic charges

One should stick to the precautionary measures also after the ESD-sensitive components have been mounted on the PCB. Until the sub-PCBs have been incorporated into a complete system on which the correct supply voltages are connected, the PCB is nothing more than an extension of the conductors of the components on this PCB. To prevent electrostatic discharges from passing to the components via the terminals, we recommend that you apply conductive clips or conductive tape on the terminals of the PCB.

3.3.7 Transients (switch-on phenomena)

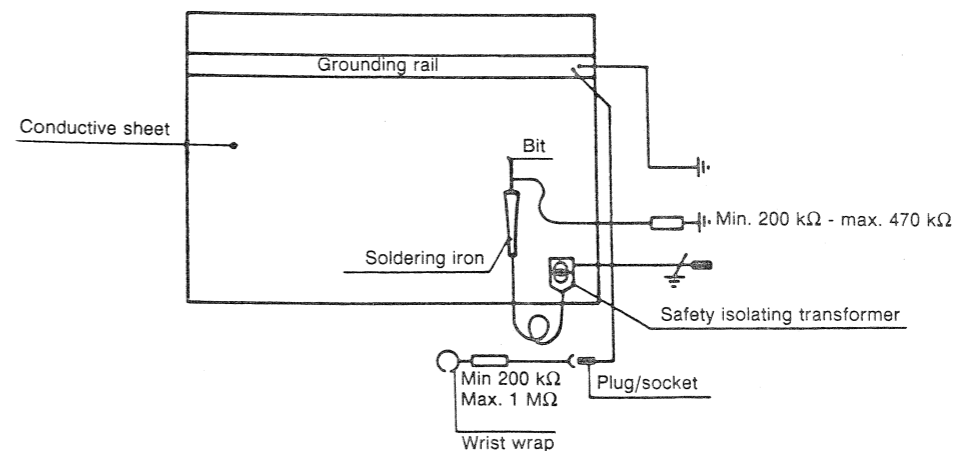
To prevent permanent damages as a result of switch-on phenomena, no ESD-sensitive components, or PCBs populated with these components, should be inserted in or removed from test-sockets or systems with the supply voltage on. Prevent switching peaks on the mains as a consequence of switching electric equipment, relay and DC lines on and off.

3.3.8 Working environment

The work bench for the service technician should look like the one shown in the figure.

3.3.9 Replacement of the Flat Pack IC's

For replacing a component see Fig. 6 Dismounting and Mounting. Also a number of precautions and examples is given. When replacing a flat pack, rosin flux applied to the device leads will ensure a good soldered joint. Since rosin flux, when not properly heated by the soldering process, is sticky, it will attract dust which will result in component degeneration over a period of time. The removal of excess flux with a cleaner will not solve this problem because the flux is then even spread over a greater area by the cleaner. Drying of the flux can be accomplished by blowing the area with a common hair dryer for 1 or 2 minutes at a distance of approx. 10 centimeters.

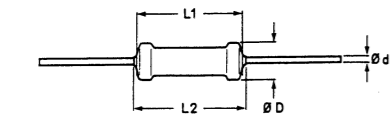


Special attention should be paid in regions having a dry atmosphere and when the floor is covered with a nylon carpet or such.

3.4 CODENUMBERS FOR STANDARDIZED RESISTORS

Unless otherwise specified, all defective resistors in the circuits of the set can be replaced by standardized types, mentioned in this chapter.

VR25, VR37 high-ohmic/high-voltage resistors



type	D _{max}	L1 _{max}	L2 _{max}	d
VR25	2,5	6,5	7,5	0,6
VR37	3,7	9,0	10,0	0,7

Range VR25 : 100 KΩ to 22 MΩ
Range VR37 : 100 KΩ to 33 MΩ

Composition of the service number for the VR25 and VR37
Main subgroup: 4822 053 20... and 4822 053 21...

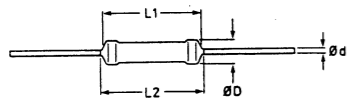
The codenumber above is completed by inserting the first two figures (resistance code) followed by the multiplier.

4 for R = 100K to 910 KΩ
5 for R = 1M to 9.1 MΩ
6 for R = or > 10M

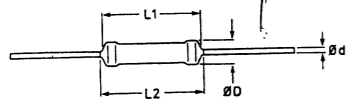
Example's:
The serv.nbr. for a VR25 resistor of 100 KΩ is 4822 053 20104
The serv.nbr. for a VR37 resistor of 33 MΩ is 4822 053 21336

PR01, PR02 and PR03 power metal film resistors

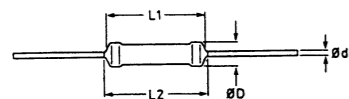
φD _{max}	L1	L2 _{max}	φd
2,5	6,5	8,0	0,6



φD _{max}	L1 _{max}	L2 _{max}	φd
3,9	10	11	0,8



φD _{max}	L1 _{max}	L2 _{max}	φd
5,2	16,7	17,9	0,8



Rated dissipation at T(amb) = 70 degrees :
PR01 = 1 Watt, PR02 = 2 Watt, PR03 = 3Watt

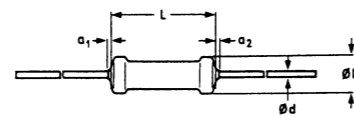
Composition of the service number for the PR01, PR02 and PR03
Main subgroup: 4822 053 10... ; 4822 053 11... and 4822 053 12...

The codenumber above is completed by inserting the first two figures (resistance code) followed by the multiplier.

8 for R= 1 to 9,1 Ω
9 for R= 10 to 91 Ω
1 for R= 100 to 910 Ω
2 for R= 1 to 9,1 KΩ
3 for R= 10 to 91 KΩ
4 for R= 100 to 910 KΩ
5 for R= or > 1 MΩ

Example:
The serv.nbr. of a PR01 resistor of 47 Ω is: 4822 053 10479
The serv.nbr. of a PR03 resistor of 1 MΩ is: 4822 053 12105

NFR25 fusible resistors



D _{max}	L _{max}	d	a1 + a2
2,5	6,5	0,6	< 1

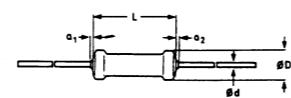
Composition of the service number for the NFR25
Main subgroup: 4822 052 10...

The codenumber above is completed by inserting the first two figures (resistance code) followed by the multiplier.

8 for R= 1 to 9,1 Ω
9 for R= 10 to 91 Ω
1 for R= 100 to 910 Ω
2 for R= 1 to 9,1 KΩ
3 for R= 10 to 91 KΩ

Example:
The service number of a resistor of 47 Ω is: 4822 052 10479

NFR25H fusible resistors



D _{max}	L _{max}	d	a1 + a2
2,5	6,5	0,8	< 1

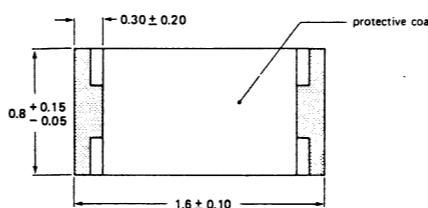
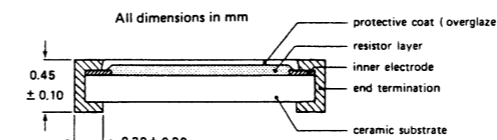
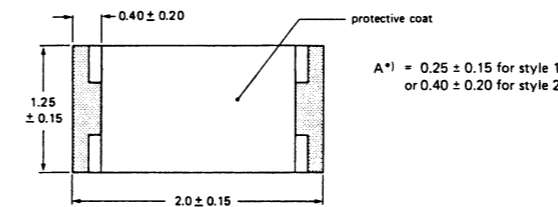
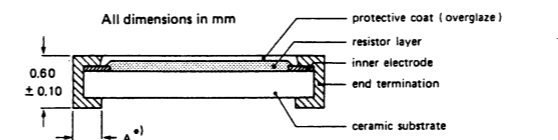
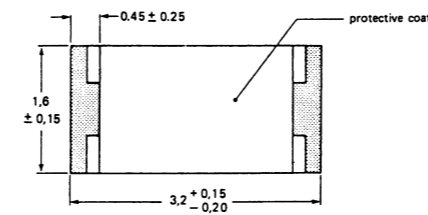
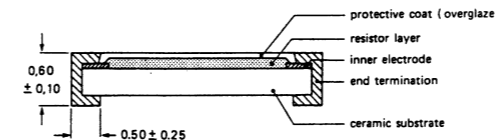
Composition of the service number for the NFR25H
Main subgroup: 4822 052 11...

The codenumber above is completed by inserting the first two figures (resistance code) followed by the multiplier.

8 for R= 1 to 9,1 Ω
9 for R= 10 to 91 Ω
1 for R= 100 to 910 Ω
2 for R= 1 to 9,1 KΩ
3 for R= 10 to 91 KΩ

Example:
The service number of a resistor of 47 Ω is: 4822 052 11479

RC-01, RC-11 AND RC-21 chip resistors



Absolute max. dissipation :
RC-01 : 0,25 W, RC-11 : 0,10 W, RC-21 : 0,062 W.

Range: RC-01 0 Ω TO 10 MΩ
RC-11 0 Ω TO 10 MΩ
RC-21 0 Ω TO 6,8 MΩ

Composition of the service number for the RC-01, RC-11 and RC-21
Main subgroup: 4822 051 10... , 4822 051 20... and 4822 051 30...
The codenumber above is completed by inserting the first two figures (resistance code) followed by the multiplier.

8 for R= 0 to 9,1 Ω
9 for R= 10 to 91 Ω
1 for R= 100 to 910 Ω
2 for R= 1 to 9,1 KΩ
3 for R= 10 to 91 KΩ
4 for R= 100 to 910 KΩ
5 for R= 1 to 9,1 MΩ
6 for R= or > 10 MΩ

The coder first three multiplier.

8 for R= 10 to 91 Ω
9 for R= 100 to 910 Ω
1 for R= 1 to 9,1 KΩ
2 for R= 10 to 91 KΩ
3 for R= 100 to 910 KΩ
4 for R= 1 to 9,1 MΩ
5 for R= or > 10 MΩ

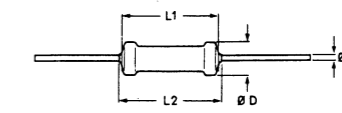
Example:
The serv. 4822 050

Example's:
The serv.nbr. for a RC-01 resistor of

0 Ω is 4822 051 10008
The serv.nbr. for a RC-11 resistor of 0 Ω is 4822 051 20008
The serv.nbr. for a RC-21 resistor of 0 Ω is 4822 051 30008

The serv.nbr. for a RC-01 resistor of 10 Ω is 4822 051 10109
The serv.nbr. for a RC-11 resistor of 10 Ω is 4822 051 20109
The serv.nbr. for a RC-21 resistor of 10 Ω is 4822 051 30109

MRS16T metal film resistors with low-inductance



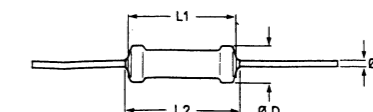
D	L	L2 _{max}	d
1,7 +0,2/-0,1	3,5 +0,2/-0,15	3,7	0,5 -0,04

Composition of the service number for the MRS16T
Main subgroup: 4822 050 1....
The codenumber above is completed by inserting the first three figures (resistance code) followed by the multiplier.

8 for R= 4,99 to 9,76 Ω
9 for R= 10 to 97,6 Ω
1 for R= 100 to 976 Ω
2 for R= 1 to 9,76 KΩ
3 for R= 10 to 97,6 KΩ
4 for R= 100 to 976 KΩ
5 for R= or > 1 MΩ

Example:
The service number of a resistor of 487 Ω is: 4822 050 14871

MRS25 metal film resistors (0,5%)

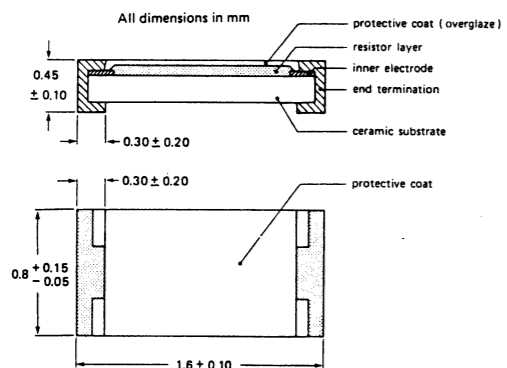
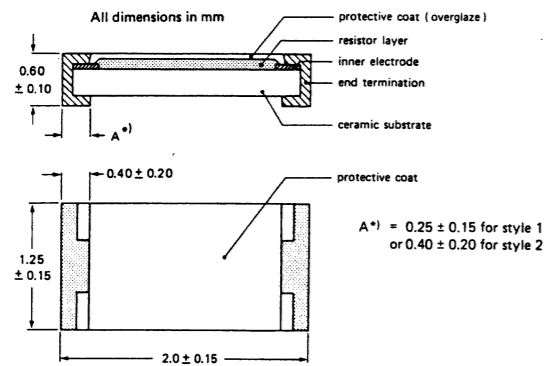
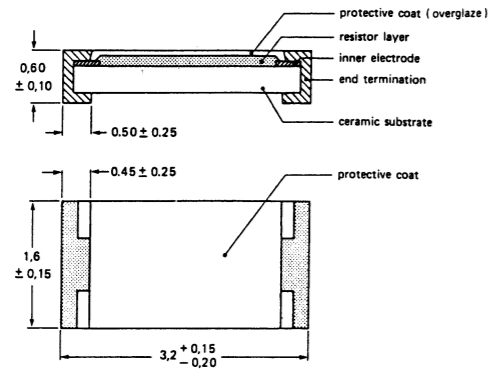


D	L1	L2 _{max}	d
2,5	6,5	7,0	0,6 ± 0,03

Composition of the service number for the MRS25
Main subgroup: 4822 050 2....

by inserting the
wed by the

RC-01, RC-11 AND RC-21 chip resistors



Absolute max. dissipation :
RC-01 : 0,25 W, RC-11 : 0,10 W, RC-21 : 0,062 W.

Range: RC-01 0 Ω TO 10 MΩ
RC-11 0 Ω TO 10 MΩ
RC-21 0 Ω TO 6,8 MΩ

Composition of the service number for the RC-01, RC-11 and RC-21
Main subgroup: 4822 051 10... , 4822 051 20... and 4822 051 30...
The codenumber above is completed by inserting the first two figures (resistance code) followed by the multiplier.

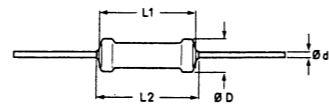
- 8 for R= 0 to 9.1 Ω
- 9 for R= 10 to 91 Ω
- 1 for R= 100 to 910 Ω
- 2 for R= 1 to 9.1 KΩ
- 3 for R= 10 to 91 KΩ
- 4 for R= 100 to 910 KΩ
- 5 for R= 1 to 9.1 MΩ
- 6 for R= or > 10 MΩ

Example's:
The serv.nbr. for a RC-01 resistor of

0 Ω is 4822 051 10008
The serv.nbr. for a RC-11 resistor of
0 Ω is 4822 051 20008
The serv.nbr. for a RC-21 resistor of
0 Ω is 4822 051 30008

The serv.nbr. for a RC-01 resistor of
10 Ω is 4822 051 10109
The serv.nbr. for a RC-11 resistor of
10 Ω is 4822 051 20109
The serv.nbr. for a RC-21 resistor of
10 Ω is 4822 051 30109

MRS16T metal film resistors with low-inductance



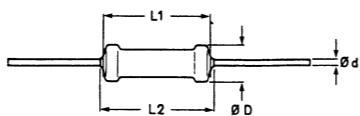
D	L	L2 max.	d
1,7 ^{+0,2} _{-0,1}	3,5 ^{+0,2} _{-0,15}	3,7	0,5 - 0,04

Composition of the service number for the MRS16T
Main subgroup: 4822 050 1....
The codenumber above is completed by inserting the first three figures (resistance code) followed by the multiplier.

- 8 for R= 4,99 to 9,76 Ω
- 9 for R= 10 to 97,6 Ω
- 1 for R= 100 to 976 Ω
- 2 for R= 1 to 9,76 KΩ
- 3 for R= 10 to 97,6 KΩ
- 4 for R= 100 to 976 KΩ
- 5 for R= or > 1 MΩ

Example:
The service number of a resistor of 487 Ω is:
4822 050 14871

MRS25 metal film resistors (0,5%)



D	L1	L2 max.	d
2,5	6,5	7,0	0,6 ± 0,03

Composition of the service number for the MRS25
Main subgroup: 4822 050 2....

The codenumber above is completed by inserting the first three figures (resistance code) followed by the multiplier.

- 8 for R= 1 to 9,76 Ω
- 9 for R= 10 to 97,6 Ω
- 1 for R= 100 to 976 Ω
- 2 for R= 1 to 9,76 KΩ
- 3 for R= 10 to 97,6 KΩ
- 4 for R= 100 to 976 KΩ
- 5 for R= 1 to 9,76 MΩ
- 6 for R= or > 10 MΩ

Example:
The service number of a resistor of 976 Ω is:
4822 050 29761

7 Ω
MΩ



or the NFR25

by inserting the
wed by the

7 Ω



r the NFR25H

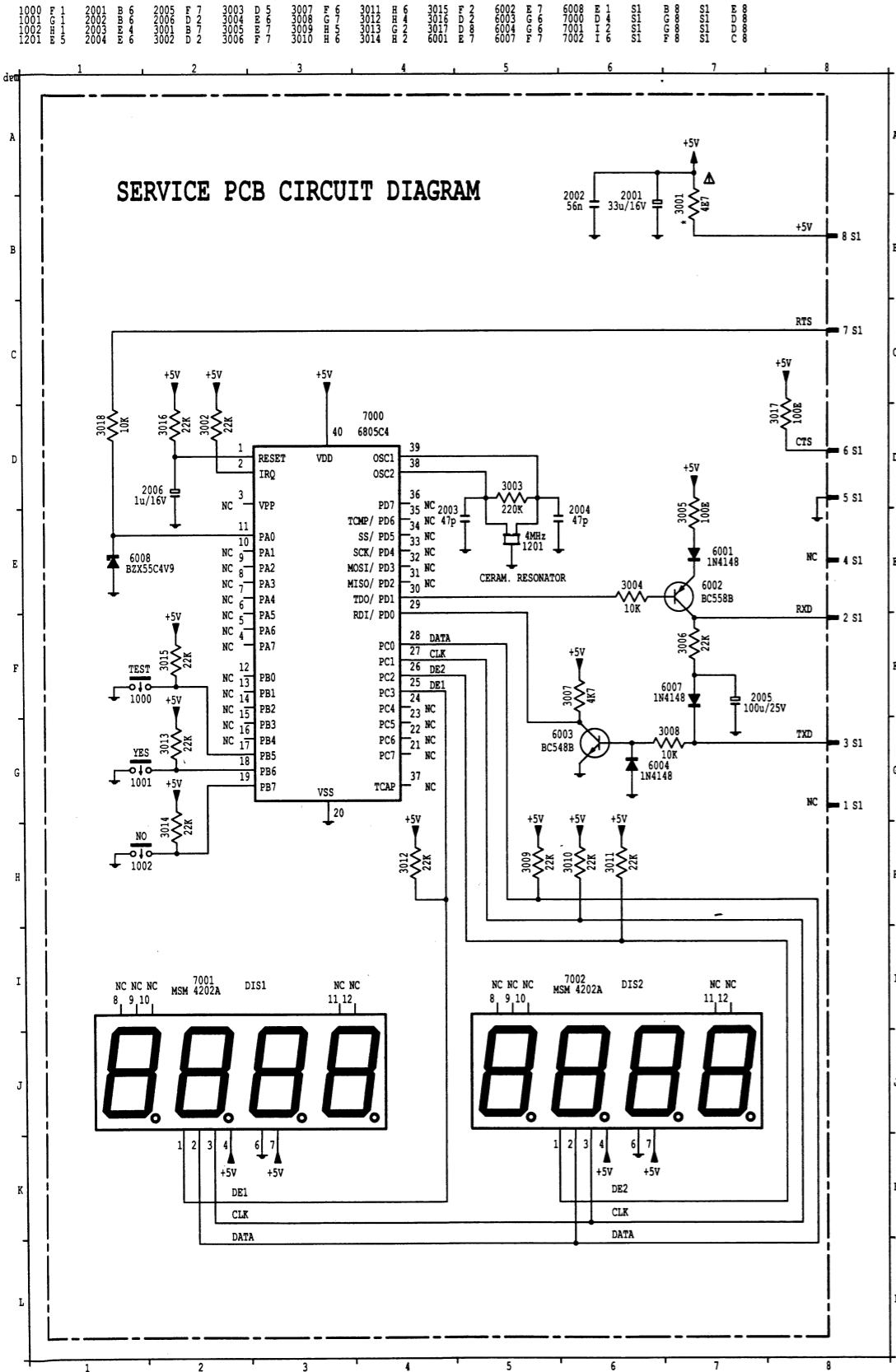
by inserting the
wed by the

7 Ω

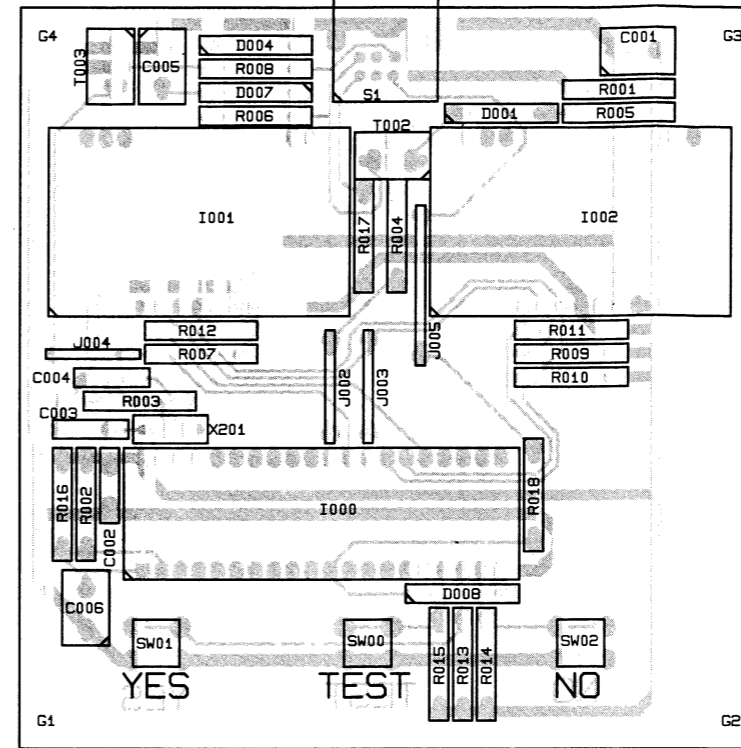
3.5 SERVICE TOOLS

3.5.1 Service PCB

3.5.1.1 Circuit diagram



3.5.1.2 Layout



3.5.1.3 Parts list

ITEM	DESCRIPTION	CODENUMBER	ITEM	DESCRIPTION	CODENUMBER	
1000	Tact switch	4822 276 10974	3010	22	KΩ	
1001	Tact switch	4822 276 10974	3011	22	KΩ	
1002	Tact switch	4822 276 10974	3012	22	KΩ	
			3013	22	KΩ	
1201	Ceram.resonator	4822 242 72527	3014	22	KΩ	
			3015	22	KΩ	
2001	33	IF/16V	4822 124 20688	3016	22	KΩ
2002	56	nF	4822 121 41154	3017	100	Ω
2003	47	pF	4822 122 31072			
2004	47	pF	4822 122 31072	6001	1N4148	4822 130 30621
2005	100	Ω	4822 124 20701	6002	BC558B	4822 130 44197
2006	1	Ω	4822 124 20722	6003	BC548B	4822 130 40937
				6004	1N1448	4822 130 30621
3001	4,7	Ω	See standardized list	6005	BZX55 C4V7	4822 130 34174
3002	22	KΩ	chapter 3.4	6006	BAT85	4822 130 31983
3003	220	KΩ		6007	1N1448	4822 130 30621
3004	10	KΩ				
3005	100	Ω		7000	MC68HC705C4	4822 900 10272
3006	22	KΩ		7001	MSM 4202A	4822 130 90474
3007	4,7	KΩ		7002	MSM 4202A	4822 130 90474
3008	10	KΩ				
3009	22	KΩ		S1	miniDIN 8pins	4822 267 31289

3.5.2 Test discs

CODE-NUMBER	NAME
4822 397 30096	Testdi (musi Testdi (musi and fi

4822 397 30155	test d 1 KHz signal
----------------	---------------------

4822 397 30184	Audio
----------------	-------

4822 701 11922	Skew
----------------	------

4822 701 11923	Excer 150 I
----------------	-------------

3.5.3 Extension connec

CODE-NUMBER	NAMI
-------------	------

4822 321 22267	10 po
----------------	-------

4822 321 22268	6 polk
----------------	--------

3.5.4 Measurement ec

Electronic Digital Multi
Digital oscilloscope
Analog oscilloscope
Timer/counter

3.5.5 Pointing devices

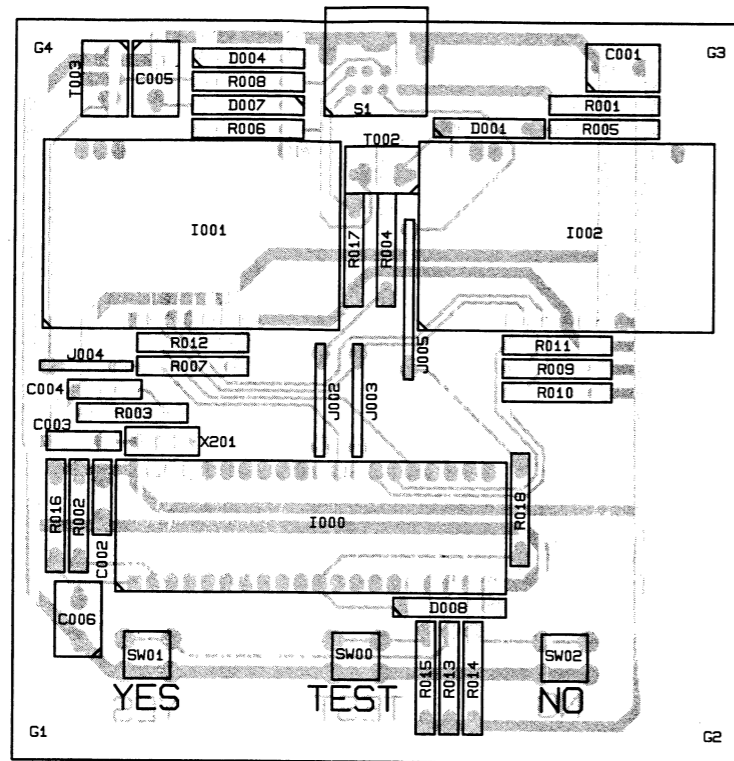
CODE-NUMBER	NAMI
-------------	------

4822 218 104 01	RV67
4822 218 104 38	RV67
4822 691 302 44	22ER

3.5.6 (de)No unting to

Torx screwd rivers

3.5.1.2 Layout



3.5.1.3 Parts list

ITEM	DESCRIPTION	CODENUMBER	ITEM	DESCRIPTION	CODENUMBER
1000	Tact switch	4822 276 10974	3010	22	KΩ
1001	Tact switch	4822 276 10974	3011	22	KΩ
1002	Tact switch	4822 276 10974	3012	22	KΩ
			3013	22	KΩ
1201	Ceram.resonator	4822 242 72527	3014	22	KΩ
2001	33 IF/16V	4822 124 20688	3015	22	KΩ
2002	56 nF	4822 121 41154	3016	22	KΩ
2003	47 pF	4822 122 31072	3017	100	Ω
2004	47 pF	4822 122 31072			
2005	100 IF/25V	4822 124 20701	6001	1N4148	4822 130 30621
2006	1 IF/63V	4822 124 20722	6002	BC558B	4822 130 44197
			6003	BC548B	4822 130 40937
			6004	1N1448	4822 130 30621
3001	4,7 Ω	See standardized list chapter 3.4	6005	BZX55 C4V7	4822 130 34174
3002	22 KΩ		6006	BAT85	4822 130 31983
3003	220 KΩ		6007	1N1448	4822 130 30621
3004	10 KΩ				
3005	100 Ω		7000	MC68HC705C4	4822 900 10272
3006	22 KΩ		7001	MSM 4202A	4822 130 90474
3007	4,7 KΩ		7002	MSM 4202A	4822 130 90474
3008	10 KΩ				
3009	22 KΩ		S1	miniDIN 8pins	4822 267 31289

3.5.2 Test discs

CODE-NUMBER	NAME/DESCRIPTION	APPLICATION
4822 397 30096	Testdisc 5 (music) Testdisc 5A (music + dropouts and fingerprints)	Reference disc for playability and adjustments of CDM
4822 397 30155	test disc with 1 KHz continous signal, 70 minutes.	life test in case of intermittent faults
4822 397 30184	Audio signals	Measure specs.
4822 701 11922	Skew disc 0,6	Reference disc for playability
4822 701 11923	Excentricity disc 150 I	Reference disc for playability

3.5.3 Extension connectors

CODE-NUMBER	NAME/DESCRIPTION	APPLICATION
4822 321 22267	10 poles ext.	For measuring Encoder panel
4822 321 22268	6 poles ext.	For measuring APU panel

3.5.4 Measurement equipment

Electronic Digital Multimeter
Digital oscilloscope
Analog oscilloscope
Timer/counter

3.5.5 Pointing devices

CODE-NUMBER	NAME/DESCRIPTION	APPLICATION
4822 218 10401	RV6701/00	Remotecntrl. /05
4822 218 10438	RV6703/00	Remotecntrl. /00
4822 691 30244	22ER9011/00	Mouse

3.5.6 (de)Mounting tool

Torx screw drivers 4822 395 50145

3.6 THE MMC CENTRAL REPAIR PROCEDURE

In case of a defect on the MMC part, the complete panel must be sent back to PCS for repair.
Below a brief description is given, a more detailed procedure is available at P.C.S Logistics Management, systems and Procedure Office.

CODENUMBER MMC:	
Version	Codenummer
/00,/05	4822 214 51981
/11	4822 214 51979
/17P	4822 214 51933
/17T	4822 214 51938

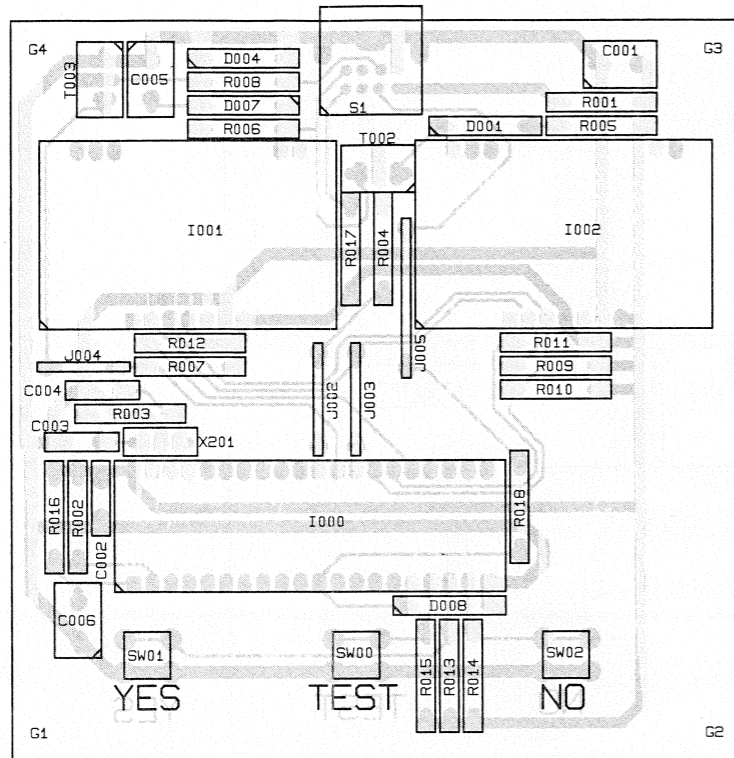
- NSO or Customer: send telex or on-line MSH system info to PCS customer relations officer with indicated number(s) and service 12NC for a repair reference number.
- PCS: send telex or MSH info with repair reference number and return invoice price. Also the same number(s) of new/repared items are sent with invoice.
- NSO or customer: send defective item(s) to PCS at SDM1 by standard address label with repair reference number and return invoice to PCS -price center.
- Remark: the difference between the invoice price and return invoice price gives the 'repair price' for the NSO
- PCS: send defective item to factory and stock.
- Experience has learned that the status of the particular products and packaging needs your local attention. Products will be returned in case of unacceptable conditions.

REPAIR PROCEDURE CONDITIONS :

- HANDLE WITH CARE IN AN ESD PROTETECTED ENVIRONMENT.
- Defective items must be sent back to PHILIPS CONSUMER SERVICE for repair forwarded by Address sticker.
- Put the address sticker properly on a free area of the box.
- Boards must not be reworked or damaged.
- Re-use original package order new package in case of damages.
- Remove additional stickers and labeling if re-using the original box.
Service codenummer on sticker must be equal to code-number on repairable item.

!!! If the above conditions are not fulfilled, hen boards are not accepted and the return price will not be credited !!!

3.5.1.2 Layout



3.5.1.3 Parts list

ITEM	DESCRIPTION	CODENUMBER	ITEM	DESCRIPTION	CODENUMBER
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3002	22	KΩ	6004	1N1448	4822 130 30621
3003	220	KΩ	6005	BZX55 C4V7	4822 130 34174
3004	10	KΩ	6006	BAT85	4822 130 31983
3005	100	Ω	6007	1N1448	4822 130 30621
3006	22	KΩ	7000	MC68HC705C4	4822 900 10272
3007	4,7	KΩ	7001	MSM 4202A	4822 130 90474
3008	10	KΩ	7002	MSM 4202A	4822 130 90474
3009	22	KΩ	S1	miniDIN 8pins	4822 267 31289

3.5.2 Test discs

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3.5.6 (de)Mounting tool

Torx screw drivers	4822 395 50145
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- NSO or Customer: send telex or on-line MSH system info to PCS customer relations officer with indicated number(s) and service 12NC for a repair reference number.
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REPAIR PROCEDURE CONDITIONS :

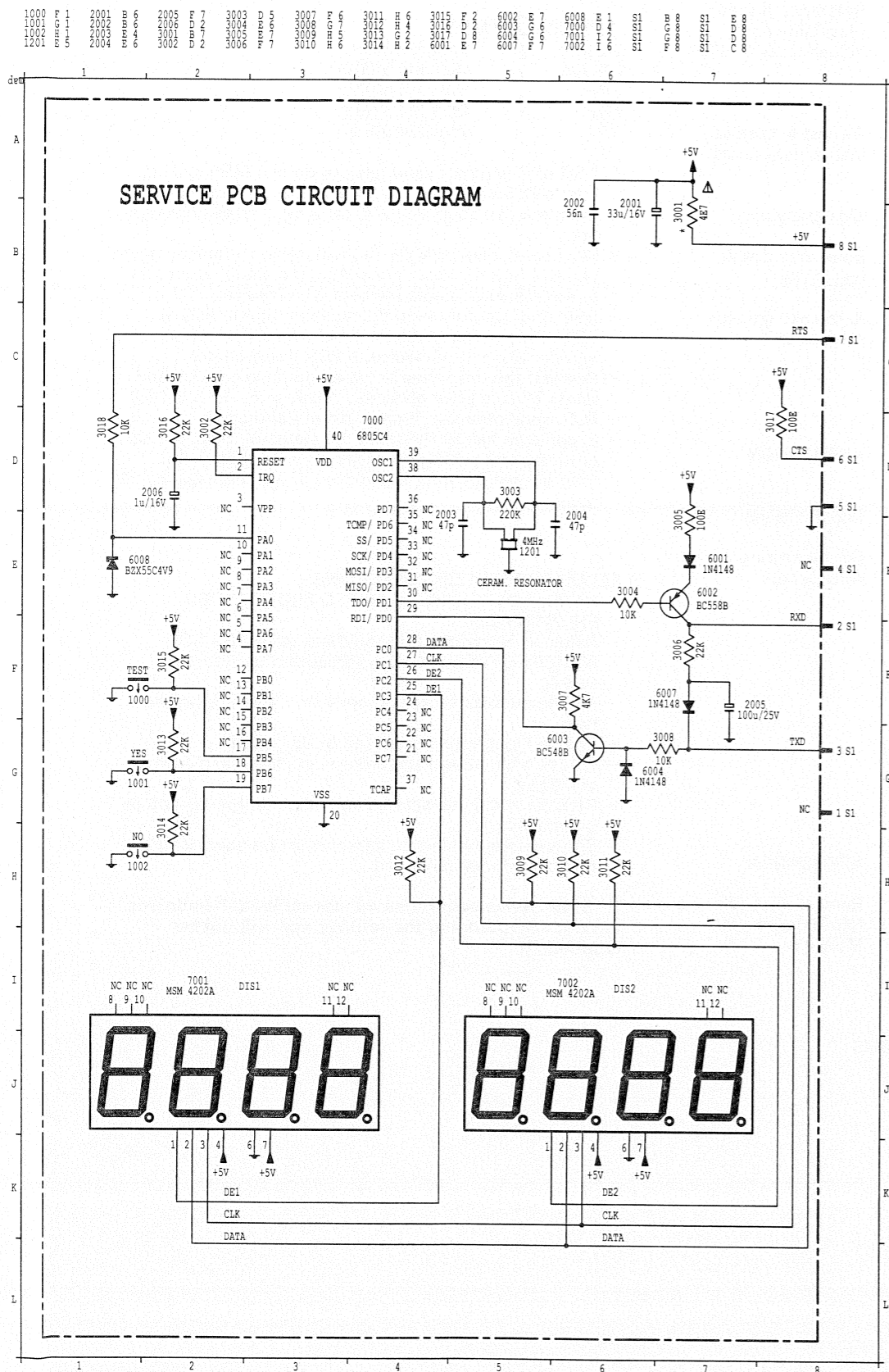
- HANDLE WITH CARE IN AN ESD PROTETECTED ENVIRONMENT.
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- Put the address sticker properly on a free area of the box.
- Boards must not be reworked or damaged.
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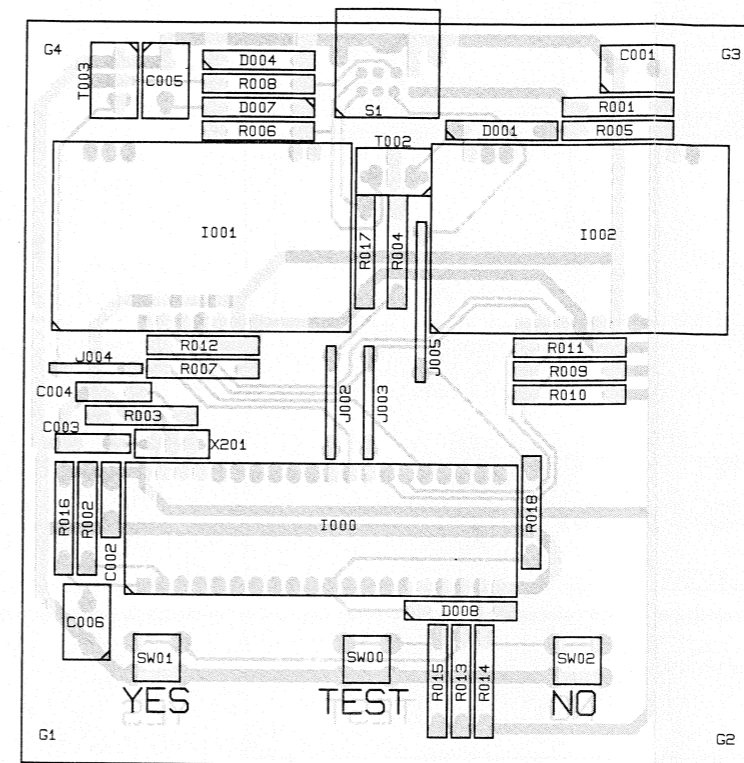
3.5 SERVICE TOOLS

3.5.1 Service PCB

3.5.1.1 Circuit diagram



3.5.1.2 Layout



3.5.1.3 Parts list

ITEM	DESCRIPTION	CODENUMBER	ITEM	DESCRIPTION	CODENUMBER	
1000	Tact switch	4822 276 10974	3010	22	KΩ	
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			3015	22	KΩ	
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2002	56	nF	4822 121 41154	3017	100	Ω
2003	47	pF	4822 122 31072			
2004	47	pF	4822 122 31072	6001	1N4148	4822 130 30621
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2006	1	IF/63V	4822 124 20722	6003	BC548B	4822 130 40937
				6004	1N1448	4822 130 30621
3001	4,7	Ω		6005	BZX55 C4V7	4822 130 34174
3002	22	KΩ		6006	BAT85	4822 130 31983
3003	220	KΩ		6007	1N1448	4822 130 30621
3004	10	KΩ				
3005	100	Ω		7000	MC68HC705C4	4822 900 10272
3006	22	KΩ		7001	MSM 4202A	4822 130 90474
3007	4,7	KΩ		7002	MSM 4202A	4822 130 90474
3008	10	KΩ				
3009	22	KΩ		S1	miniDIN 8pins	4822 267 31289

3.5.2 Test discs

CODE-NUMBER	NAME	DESC
4822 397 30096	Testdi	(musi
	Testdi	(musi
	and fi	
4822 397 30155	test d	1 KHz
	signal	
4822 397 30184	Audio	
4822 701 11922	Skew	
4822 701 11923	Excer	150 l

3.5.3 Extension conne

CODE-NUMBER	NAMI	DESC
4822 321 22267	10 po	
4822 321 22268	6 pol	

3.5.4 Measurement ec

Electronic Digital Multi
Digital oscilloscope
Analog oscilloscope
Timer/counter

3.5.5 Pointing devices

CODE-NUMBER	NAMI	DESC
4822 218 104 01	RV67	
4822 218 104 38	RV67	
4822 691 31244	22ER	

3.5.6 (de)Mounting to

Torx screw d rivers

4 MECHANICAL DRAWINGS AND PARTS LIST

4.1 DEMOUNTING INSTRUCTIONS OF CABINET

NOTE: Numbers in parenthesis () refer to the Exploded View reference numbers.

4.1.1 Top Cover Removal (216)

Remove the four Top Cover screws on both sides of the unit.

4.1.2 Front Assembly Removal (202)

Remove the Top Cover, refer to section 4.1.1.

Remove the CDM Tray Front assembly (203) by opening the CDM Drawer and lifting the CDM Tray Front Assembly up. Remove the three front screws on the top of the Front Assembly and the three front screws on the bottom of the front assembly. Remove the two top front frame corner screws located directly behind the Front Assembly top corner screws.

Note: By removing the two top front frame corner screws, the two bottom Front assembly clips will disengage from the bottom of the Front Frame Bracket (502) Carefully angle the top of the Front Assembly and slide the Front Assembly Cover off of the unit. Remove the two screws of the HP Panel (1007) mounting bracket. Disconnect the two connectors on the Display panel (1005).

Note: Connectors are removed from connector sockets by releasing the socket connector clips. Remove the Power Switch Connector Shaft (522) by pulling it forward out of Front Frame Bracket (502).

4.1.3 Display Panel Removal (1005)

Remove the Top Cover, refer to section 4.1.1.

Remove the Front Assembly, refer to section 4.1.2.

Remove the seven screws attaching the Display Panel to the Front Assembly (202)

4.1.4 Power Supply Panel Removal (1006)

Remove the Top Cover, refer to section 4.1.1.

Remove the Rear Textplate (513) by removing the four screws. Remove the two Power Supply mounting screws on the Rear Frame Bracket (514).

Remove the two Power Supply mounting screws on the Right Frame Bracket (518).

Note: The two Power Supply screws secured to the Right Frame Bracket are mounted to a heatsink on the Power Supply Panel. Be careful not to damage the Power Supply Panel when disassembling or assembling.

Remove the Power Supply mounting screw located on the top front of the Power Supply Bracket (517). Remove the power switch connecting cable from the Cord Clamps (504, 508). Lift the front of the Power Supply Panel up two inches and remove the two connectors. Slide the power Supply Panel out toward the front of the unit. Disconnect the remaining connector.

4.1.5 APU panel & Encoder Panel (1002, 1003).

Remove the Top Cover, refer to section 4.1.1.

Note: The APU Panel and Encoder Panel are attached to the CD Panel (1004) by two PCB connectors for each Panel. Both panels are also secured in place by guides that protrude from both the Left Frame Bracket (506).

Remove all wire connectors attached to the Panels and carefully lift each panel up out of the PCB connectors.

4.1.6 CDM Loader Assembly Removal (212)

Note: The laser diode is extremely sensitive to static electricity.

Before Removing the CDM Loader Assembly, properly ground yourself using a Wrist Grounding Strap.

Remove the Top Cover, refer to section 4.1.1.

Remove the Front Assembly, refer to section 4.1.2.

Open the CDM Drawer and remove the two front mounting screws. Remove the rear mounting screw. Lift the front of the CDM Loader Assembly one inch and locate the CDM flat cable and flat cable socket. Lift the top of the socket to release the cable, pull the cable up from the connector and immediately attach a paper clip to the bare ends of the flat cable. This procedure will insure against static electricity damage. Remove the two remaining connectors.

Note: The following numbers in parenthesis () refer to the reference numbers of the Loader Exploded View.

4.1.7 CDM Loader Disassembly.

Refer to detail 1 of the Loader Exploded View.

Note: The laser diode is extremely sensitive to static electricity.

Before removing the CDM, properly ground yourself using a Wrist Grounding Strap.

4.1.7.1 Tray Removal.

Refer to Detail 2 on the Loader Exploded View.

Remove the Top Cover, refer to section 4.1.2

Remove the Front Assembly, refer to section 4.1.6

Position the CDM Loader Assembly (1) upside down with the front of the Tray (2) facing you. Pull the Tray (2) out of its full extension.

Locate the Cover (4) and the tab protruding from the CDM Loader Assembly (1). Carefully press the Cover (4) down so that the lip on the Cover slides beneath the tab protruding from the Chassis Assembly. Slide the Cover (4) away from the tab.

Position the CDM Loader Chassis Assembly face up with the front of the Tray (2) facing you. Locate the clip and tab on the CDM Loader Chassis Assembly (1). With a small flat screwdriver, gently press the clip away from the tab protruding from the CDM Loader Tray (2). Pull the Tray (2) out of the CDM Loader Chassis Assembly.

4.1.7.2 CDM Assembly Removal (20)

Remove the Top Cover, refer to section 4.1.1

Remove the Front Assembly, refer to section 4.1.2

Remove the CDM Loader Assembly, refer to section 4.1.6

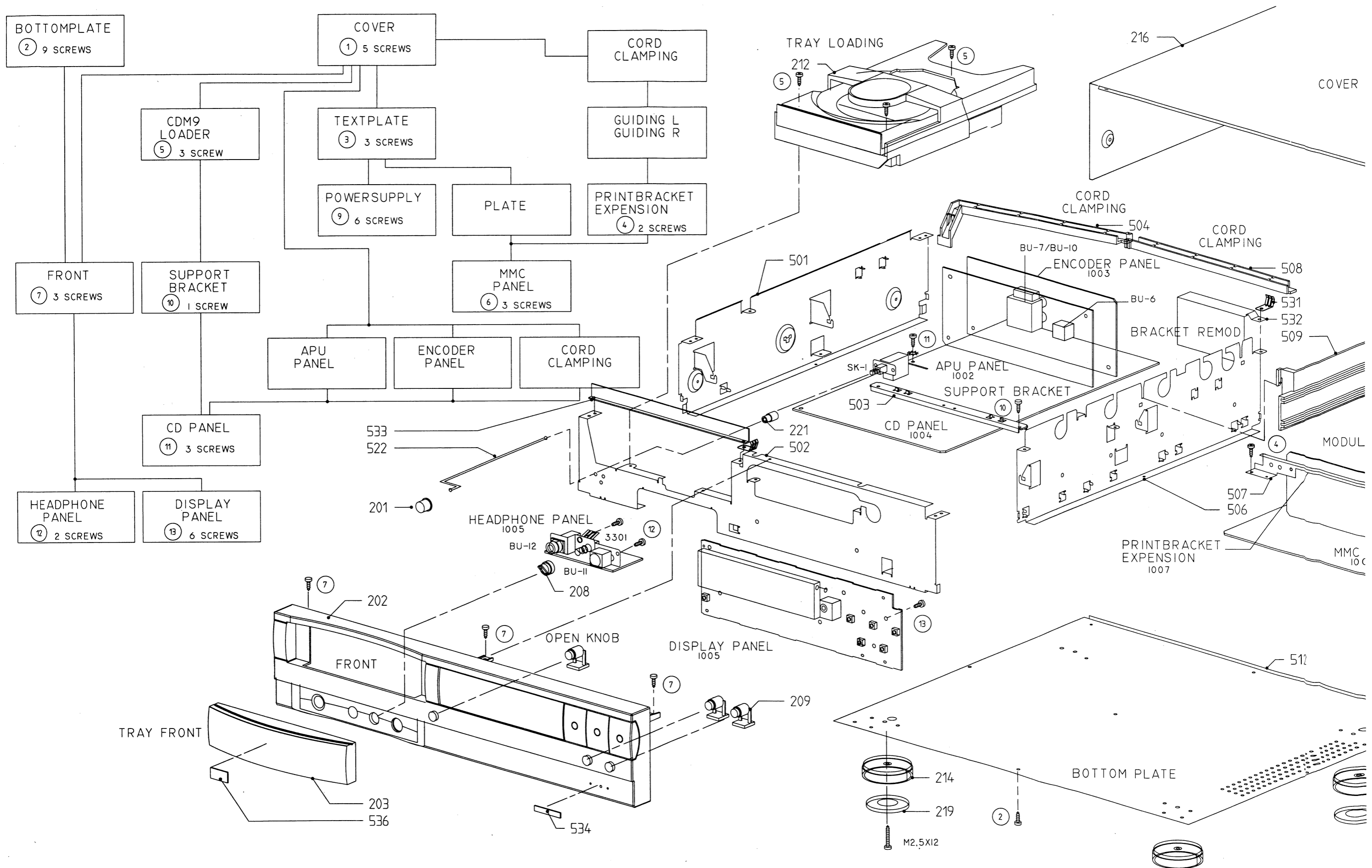
Remove the Tray, refer to section 4.1.7.1

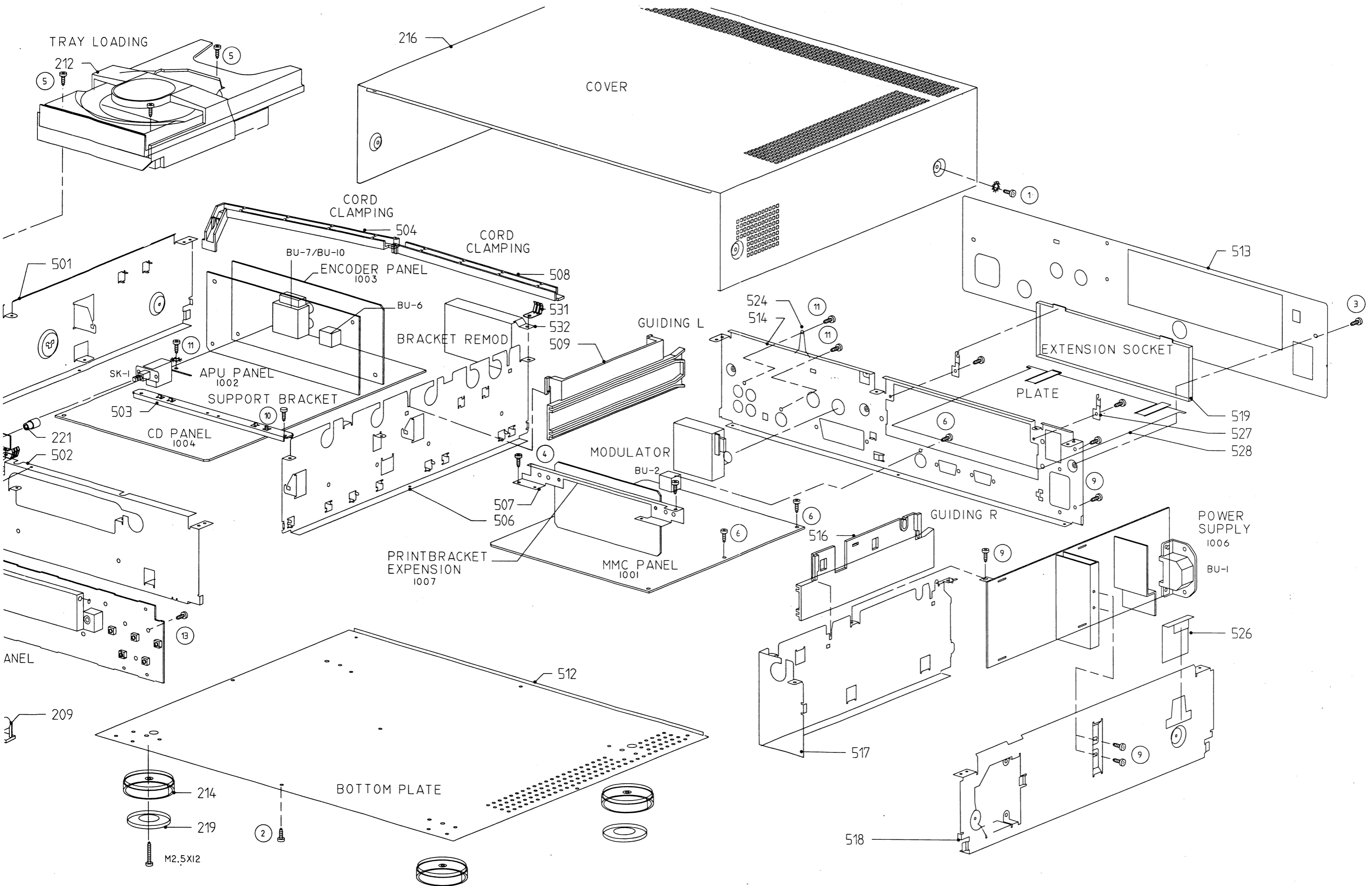
Position the CDM Loader Chassis Assembly (1) with the Motor Assembly (11) facing away from you.

Note: The CDM Assembly (20) is positioned within the CDM Loader Assembly (1) on slide tracks.

Pull the CDM Assembly (20) toward you until it reaches its slide stops. Gently lift the CDM Assembly until the slide tab is out of the slide and pull the CDM Assembly out.

4.1.8 EXPLODED VIEW OF THE CABINET

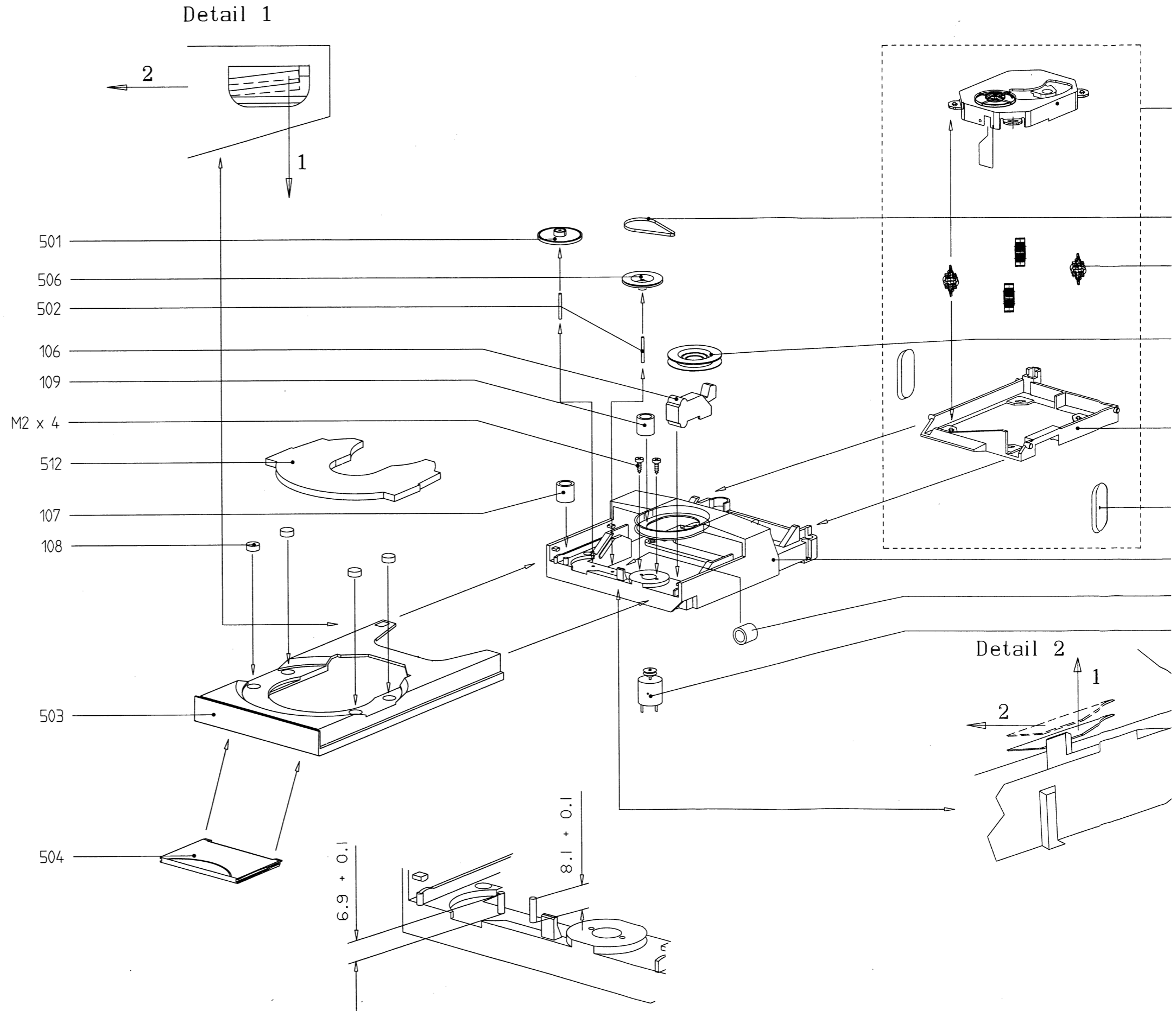




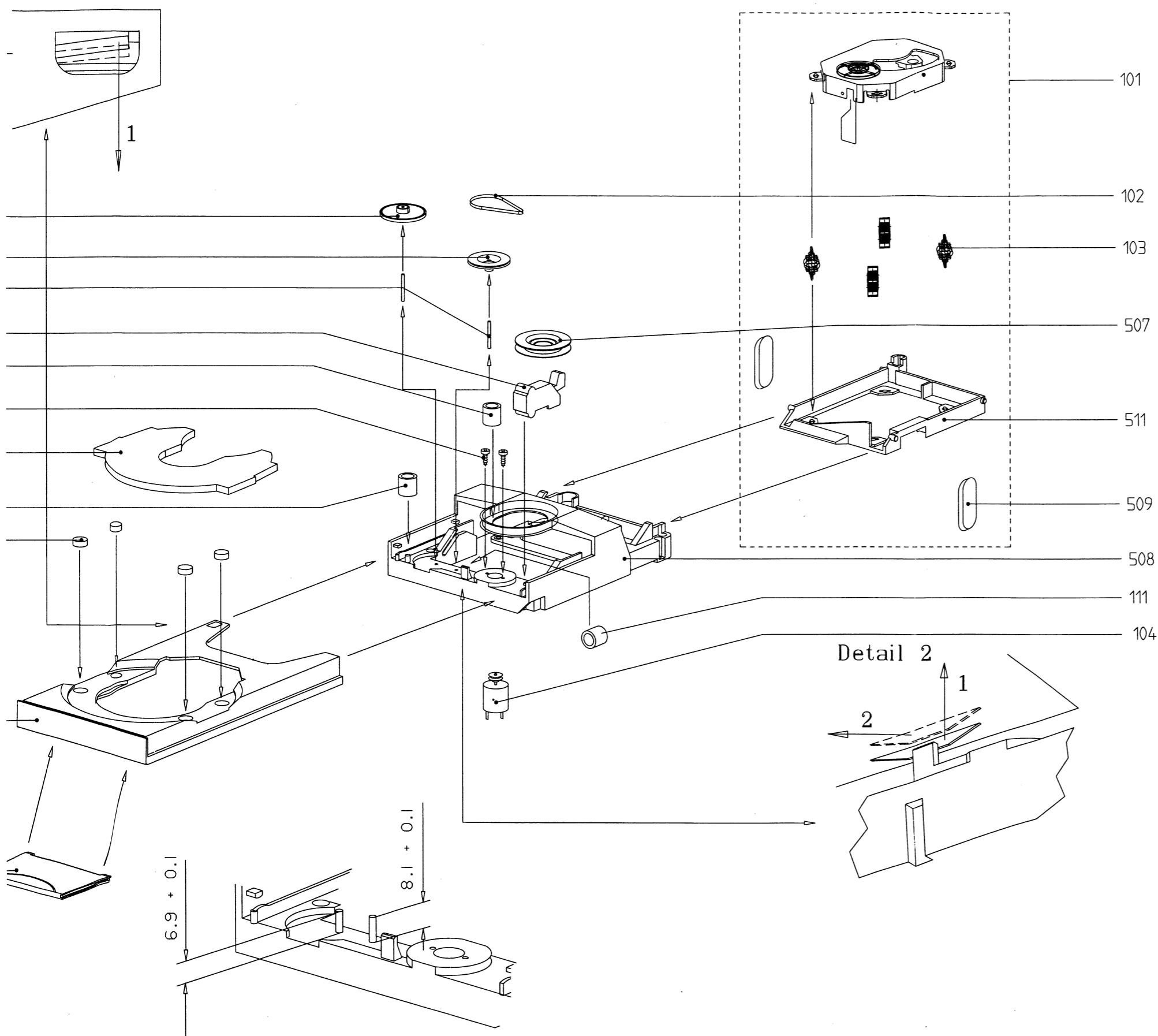
4.2 EXPLODED VIEW OF LOADER

4.1.8.1 Parts list of cabinet

201	4822 410 61721	POWER KNOB
202	4822 444 40521	FRONT ASSY
203	4822 444 40522	TRAYFRONT
208	4822 411 61674	VOLUME KNOB
214	4822 462 41895	FOOT
216	4822 444 60811	COVER ASSY
219	4822 466 93071	PLATE FOR FOOT
221	4822 535 93284	CONNECTING ROD
504	4822 401 11388	CORD CLAMPING
508	4822 401 11387	CORD CLAMPING
	4822 321 10844	MAINS CORDSET/00
RC	4822 218 10401	REMOTECONTROL FOR /05
RC	4822 218 10438	REMOTECONTROL FOR /00
SK1	4822 276 11309	MAINS POWER SWITCH
BU-2	4822 267 31289	PORT2 SOCKET
BU-6	4822 267 40857	MINIDIN VIDEO SOCKET
BU-7/		
BU-10	4822 267 20414	4P CINCH SOCKET
BU-11	4822 267 31289	PORT1 SOCKET
BU-12	4822 267 30743	HEADPHONE SOCKET
1007	4822 214 51994	FMV EXPANSION INTERFACE-PANEL
1009	4822 214 51996	MODULATOR /05
	4822 736 21426	DIRECTION FOR USE



Detail 1



4.2.1 Parts list of LOADER

103	4822 466 93065	SUSPENSION
106	4822 276 13222	SWITCH ASSY
104	4822 361 21492	MOTOR ASSY
506	4822 528 81465	PULLEY
507	4822 528 81464	DRIVE PULLEY
102	4822 358 31168	DRIVE BELT
512	4822 466 62109	TRANSPORT PROTECTION
108	4822 462 41902	ORNAMENTAL TULE
107	4822 325 80491	TULE
109	4822 325 60379	DAMPING GROMMET
109	4822 325 60379	DAMPING GROMMET
101	4822 691 30277	CDM9 ON MOUNT.CHASSY

5 SERVICE SOFTWARE

5.1 THE LOW LEVEL MMC TEST

Scope

This test is standard implemented in the boot software of CD-RTOS. It doesn't need a lot of hardware to run. When debugging or servicing an MMC panel this test is very useful.

General

This test is developed for service and low level hardware debugging purposes only. It is meant to be used with the service pcb as described in TOOLS (please refer to section 3.5 SERVICE TOOLS). The test executed with the service pcb is called the "pcb low level test". The test executed with the VT100 terminal is called the "terminal low level test". Since this service pcb display has just 8 digits, only the most important information will be displayed to the user. For the VT100 terminal this is never a problem.

This test consists out of the following items:

- a. Display header and release number.
- b. VSC
- c. ROM
- d. NVRAM
- e. DRAM
- f. CDIC
- g. SLAVE processor (68HC05)

5.1.1 Tools

In this test the service pcb acts as some kind of a 'micro terminal'. This means that the service pcb is able to display some alphabetical and numerical characters. Some characters because it uses 7-segment displays

The three keys available are:

- TEST ; test all display leds.
- Yes ; Send an ASCII 'Y'.
- No ; Send an ASCII 'N'.

The communication parameters are fixed at: 9600 baud
8 data bits
1 stopbit
no parity

The microcontroller is programmed with software available at IMS CDI software group.
The circuit diagram is on section 3.5.1.1

5.1.2 Testsequence

Table 1 below shows all the steps of the testprogram and what kind of tests are performed.

STEP	ACTION/TEST PERFORMED
00	VSC master/slave init
01	ROM
05	NVRAM
06	DRAM BANK0 & BANK1
07	DRAM BANK0
08	DRAM BANK1
09	CDIC
10	SLAVE
11	CLOCK CALIBRATION

Table 1: teststeps low level test

5.1.3 Low level test implementation

The low level test (short: lltest) is implemented in the boot part of the CD-RTOS software. The whole test occupies about 10k of ROM memory and is written in assembler.

The test runs without the use of any external RAM. It only uses internal CPU registers. As communication channel the 68070's UART is used. Before starting the normal player boot the following sequence is executed:

1. Initialize the 68070's UART : 9600 baud
 - 1 startbit
 - 8 databits
 - 1 stopbit
 - no parity
 - no handshake !
2. Clear the RXD buffer.
3. Wait 5 ms.
4. Read the RXD buffer.
5. If the character received was an ACK (\$06) the start the pcb lltest

The UART is connected to I/O port 2

5.1.4 How to start up the low level test

With service pcb

To startup the **pcb low level testsoftware** the next sequence should be followed:

- Switch off the player.
- Connect service pcb to port 2 at the rear of the player.
- Switch on the player.
- The service pcb display should now show 'CDI RLxx'. (with xx the release number)
- The pcb lltest is now ready to go.

With VT100 terminal

To startup the **terminal low level testsoftware** one should follow the next sequence:

- Switch off the player.
- Connect the terminal to the 68070's UART of the player.
- Switch on the player while pressing the SPACE-bar of the terminal.
- The terminal should now show the title of the terminal lltest.

5.1.5 PCB low level test

If the service pcb is connected to port 2 the pcb low level test is executed after power on. In table 1 a survey is given for all tests executed.

Display lltest release number:

When this lltest is entered, first the release number of the pcb lltest will be displayed.

Example: CDI RLxx

(RL stands for RELEASE, xx stands for release x.x).
The lltest is now waiting for an action from the user. The user should now press either the 'Y' or 'N' button to continue the test.

STEP 0: VSC

STEP 0A: VSC MASTER

display: 0A

In this step some registers of the VSC MASTER are initialized. These registers are :

- DCR2 register(set to independant
- DCR register (disable display)
- CSR register (set DTACK delay and DRAM type)

STEP 0B: VSC SLAVE

display: 0B

In this step some registers of the VSC SLAVE are initialized. These registers are:

- DCR2 register(set to independant DCA)
- DCR register (disable display)
- CSR register (set DTACK delay and DRAM type)

STEP 1: ROM

In this step the contents of the ROM is checked. Following tests are done on the ROM:

1. Display release number of this ROM. (test A)
3. Check if the parity of the ROM is OK. (test C)

Address range:

- The ROM chips used for this memory map are :
1 X 4Mbit.

On the MINI MMC the clock and calendar chip used is the SGS-Thomson MK48T08B. It is visible in the memory map.

Nr.of Bytes Words	UPPER --- LOWER	MAPPED ADDRESS SPACE	UNMAPPED ADDRESS SPACE	FUNCTION
512kB	UP&LO	00 0000 - 07 FFFF	00 0000 - 07 FFFF	DRAM BANK1
512kB	UP&LO	08 0000 - 0F FFFF	08 0000 - 0F FFFF	DRAM BANK2
512kB	UNDEF	10 0000 - 17 FFFF	10 0000 - 17 FFFF	RESERVED
512kB	UP&LO	18 0000 - 1F FBFF	18 0000 - 1F FBFF	SYSTEM ROM
16B	LO	1F FC00 - 1F FFBF	1F FC01 - 1F FC1F	DUART (4)
16B*	UP&LO	1F FFC0 - 1F FFDF	1F FFC0 - 1F FFDF	VCS REGS SLAVE
16B*	UP&LO	1F FFE0 - 1F FFFF	1F FFE0 - 1F FFFF	VSC REGS MASTER
4B	LO	20 0000 - 20 7FFF	20 0001 - 20 0007	SLAVE
500kB	UNDEF	20 8000 - 27 FFFF	20 8000 - 27 FFFF	FREE SPACE
64kB	LO	28 0000 - 28 FFFF	28 0001 - 28 FFFF	FLOPPY (4)
460kB	UNDEF	28 0000 - 2F FFFF	28 0000 - 2F FFFF	FREE SPACE
8kW	UP&LO	30 0000 - 30 FFFF	30 0000 - 30 3FFE	CDI
910kB	UNDEF	31 0000 - 3E FFFF	31 0000 - 3E FFFF	FREE SPACE
2B	LO	3F 0000 - 3F 7FFF	3F 0001 - 3F 0003	KILLME/DMAMEM
8KB-8	UP	3F 8000 - 3F FBFF	3F 8000 - 3F BFEE	NVRAM (2)
8B	UP	3F BFF0 - 3F FBFF	3F BFF0 - 3F BFEE	CLOCK&CAL REGS
1kB	UNDEF	3F FC00 - 3F FFFF	3F FC00 - 3F FFFF	DO NOT ACCESS(3)
13MB	UNDEF	40 0000 - FF FFFF	40 0000 - FF FFFF	EXTENSION SPACE

Table of the memory map

- (1) The effective memory space for SYSTEM ROM is 512kB-1k.
- (2) The maximum available NVRAM space in this configuration is 31 kByte.
- (3) This part of the memory map should not be accessed. The VSC registers are mapped here.
- (4) When used.

1.. Explanation of items in tables

Nbr. of Bytes/Words :
The total available bytes or words. Words in this case means the part of the memory map is only accessible as a word.

- kB = kilobytes
- B = bytes
- B* = bytes, but some addresses are only accessible as words.
- kW = kilowords, only accessible as a word!

UPPER - LOWER:

This column gives an accessible.

UP = only accessible the databus. (DATA8-DATA

LO = only accessible the databus. (DATA0-DATA

UP&LO = accessible via the databus. (the device u

UNDEF = not defined.

MAPPED ADDRESS SP

This column gives the t described in FUNCTION device can occur sever

UNMAPPED ADDRESS

Analogous as mapped ; occur only ONE time.

FUNCTION: This column

STEP 1: ROM 10

STEP 1A: ID AND RELE.

display: 1A
IDxxRLyy

In this step the release for a moment. (ID stands for IDentifica RL stands for RELEASE.

STEP 1C: CHECKSUM

display: 1C

In this step the checksu described in " how is th checksum is not ok an e

display: 1CEr05

STEP 5: NVRAM

The nvram test is a non the original nvram cont. Address range: Full nvr spec)

display: 5

- The following actions te
1. read byte from nvram
 2. write a pattern (from
 3. read byte from nvram
 4. if byte read is ok the error message and s'

If error,

display: 5 E09

5. write inverted pattern
6. read byte from nvram
7. if byte read is ok the error message and s'

If error,

display: 5 E10

8. repeat this for every

STEP 1: ROM

In this step the contents of the ROM is checked.

Following tests are done on the ROM:

1. Display release number of this ROM. (test A)
3. Check if the parity of the ROM is OK. (test C)

Address range:

- The ROM chips used for this memory map are :
1 X 4Mbit.

On the MINI MMC the clock and calendar chip used is the SGS-Thomson MK48T08B. It is visible in the memory map.

Nr.of Bytes Words	UPPER --- LOWER	MAPPED ADDRESS SPACE	UNMAPPED ADDRESS SPACE	FUNCTION
512kB	UP&LO	00 0000 - 07 FFFF	00 0000 - 07 FFFF	DRAM BANK1
512kB	UP&LO	08 0000 - 0F FFFF	08 0000 - 0F FFFF	DRAM BANK2
512kB	UNDEF	10 0000 - 17 FFFF	10 0000 - 17 FFFF	RESERVED
512kB	UP&LO	18 0000 - 1F FBFF	18 0000 - 1F FBFF	SYSTEM ROM
16B	LO	1F FC00 - 1F FFBF	1F FC01 - 1F FC1F	DUART (4)
16B*	UP&LO	1F FFC0 - 1F FFDF	1F FFC0 - 1F FFDF	VCS REGS SLAVE
16B*	UP&LO	1F FFE0 - 1F FFFF	1F FFE0 - 1F FFFF	VSC REGS MASTER
4B	LO	20 0000 - 20 7FFF	20 0001 - 20 0007	SLAVE
500kB	UNDEF	20 8000 - 27 FFFF	20 8000 - 27 FFFF	FREE SPACE
64kB	LO	28 0000 - 28 FFFF	28 0001 - 28 FFFF	FLOPPY (4)
460kB	UNDEF	28 0000 - 2F FFFF	28 0000 - 2F FFFF	FREE SPACE
8kW	UP&LO	30 0000 - 30 FFFF	30 0000 - 30 3FFE	CDI
910kB	UNDEF	31 0000 - 3E FFFF	31 0000 - 3E FFFF	FREE SPACE
2B	LO	3F 0000 - 3F 7FFF	3F 0001 - 3F 0003	KILLME/DMAMEM
8kB-8	UP	3F 8000 - 3F FBFF	3F 8000 - 3F BFEE	NVRAM (2)
8B	UP	3F BFF0 - 3F FBFF	3F BFF0 - 3F BFFE	CLOCK&CAL REGS
1kB	UNDEF	3F FC00 - 3F FFFF	3F FC00 - 3F FFFF	DO NOT ACCESS(3)
13MB	UNDEF	40 0000 - FF FFFF	40 0000 - FF FFFF	EXTENSION SPACE

Table of the memory map

- (1) The effective memory space for SYSTEM ROM is 512kB-1k.
- (2) The maximum available NVRAM space in this configuration is 31 kByte.
- (3) This part of the memory map should not be accessed. The VSC registers are mapped here.
- (4) When used.

I. Explanation of items in tables

Nbr. of Bytes/Words :

The total available bytes or words. Words in this case means the part of the memory map is only accessible as a word.

kB = kilobytes

B = bytes

B* = bytes, but some addresses are only accessible as words.

kW = kilowords, only accessible as a word!

UPPER - LOWER:

This column gives an indication of how the device is accessible.

UP = only accessible as byte via the UPPER byte of the databus.
(DATA8-DATA15)

LO = only accessible as byte via the LOWER byte of the databus.
(DATA0-DATA7)

UP&LO = accessible via LOWER as well as UPPER byte of the databus.
(the device uses the complete databus.)

UNDEF = not defined.

MAPPED ADDRESS SPACE:

This column gives the total address range where the device described in FUNCTION is accessible. In this range the device can occur several times.

UNMAPPED ADDRESS SPACE:

Analogous as mapped address space, only the device can occur only ONE time.

FUNCTION: This column describes the device or register

STEP 1: ROM 10

STEP 1A: ID AND RELEASE NUMBER DISPLAY

display: 1A
IDxxRLyy

In this step the release number of this ROM is displayed for a moment.

(ID stands for IDentification, xx is the id number. RL stands for RELEASE, yy stands for y.y)

STEP 1C: CHECKSUM

display: 1C

In this step the checksum of this ROM is calculated as described in " how is the checksum calculated ". If the checksum is not ok an error will be displayed.

display: 1C Er05

STEP 5: NVRAM

The nvram test is a non destructive test. This means that the original nvram contents is restored again.

Address range: Full nvram address range (see product spec)

display: 5

The following actions take place in the nvram test:

1. read byte from nvram and save it in a register
2. write a pattern (from ROM) to nvram
3. read byte from nvram and compare with pattern
4. if byte read is ok then continue with action 5 else give error message and stop testing

If error,

display: 5 Er09

5. write inverted pattern to nvram

6. read byte from nvram and compare with pattern

7. if byte read is ok then restore original byte else give error message and stop testing

If error,

display: 5 Er10

8. repeat this for every possible nvram address

STEP 6-8 :DRAM

The dram test is always a destructive test. The test is performed for both ram bank0 and bank1 as one large memory followed by a test for each bank separately. On the displays following, the 'x' is a memory counter. The counter is incremented every 128k. So for the full range it counts from 1 to 8.

Address range: full address range (see table)

Bank0 = lower RAM bank

Bank1 = upper RAM bank

STEP 6A : TEST THE FULL DRAM MEMORY

The following actions take place in this test:

1. fill the memory with the long word address as data.

display: 6Afx

2. read the memory contents and compare with the address.

display: 6Arx

3. if the long word read is ok then continue else give error message and stop testing.
If error,

display: 6ArxEr11

STEP 6B : TEST THE FULL DRAM MEMORY WITH INVERTED DATA

The following actions take place in this test:

1. fill the memory with the inverted long word address as data.

display: 6Bfx

2. read the memory contents and compare with the inverted address.

display: 6Brx

3. if the long word read is ok then continue else give error message and stop testing.
If error,

display: 6BrxEr12

STEP 7A : TEST DRAM BANK0

The following actions take place in this test:

1. fill the memory with the long word address as data.

display: 7Afx

2. read the memory contents and compare with the address.

display: 7Arx

3. if the long word read is ok then continue else give error message and stop testing.
If error,

display: 7ArxEr13

STEP 7B : TEST DRAM BANK0 WITH INVERTED DATA

The following actions take place in this test:

1. fill the memory with the inverted long word address as data.

display: 7Bfx

2. read the memory contents and compare with the inverted address.

display: 7Brx

3. if the long word read is ok then continue else give error message and stop testing.
If error,

display: 7BrxEr14

STEP 8A : TEST DRAM BANK1

The following actions take place in this test:

1. fill the memory with the long word address as data.

display: 8Afx

2. read the memory contents and compare with the address.

display: 8Arx

3. if the long word read is ok then continue else give error message and stop testing.
If error,

display: 8ArxEr15

STEP 8B : TEST DRAM BANK1 WITH INVERTED DATA

The following actions take place in this test:

1. fill the memory with the inverted long word address as data.

display: 8Bfx

2. read the memory contents and compare with the inverted address.

display: 8Brx

3. if the long word read is ok then continue else give error message and stop testing.
If error,

display: 8BrxEr16

STEP 9: CDIC

This test only checks part of the CDIC ram, mainly because it is possible that during the test the CDIC destroys part of the ram contents.

address range: CDIC base address + \$1400 to CDIC base address + \$3C7F.

cdic register2: CDIC base address + \$3FFA
register2 contents after reset: \$C7FE

See table for base address.

STEP 9A :CDIC RAM TEST WITH ADDRESS AS DATA

display: 9A

The following actions take place in the CDIC RAM test:

1. Fill the memory with long word address as data.
2. Read and compare the data with the address.
3. If the long word read is ok then continue else give an error and stop testing.
If error,

display: 9A Er17

STEP 9B :CDIC RAM TEST WITH INVERTED ADDRESS AS DATA

display: 9B

The following actions take place in the CDIC RAM test:

1. Fill the memory with inverted long word address as data.
2. Read and compare the data with the inverted address.
3. If the long word read is ok then continue else give an error and stop testing.
If error,

display: 9A Er18

STEP 9C :CDIC REGISTER 2 TEST

display: 9C

The following actions take place in the CDIC REGISTER test:

1. Read register 2 and compare with fixed pattern. (Register 2 has a defined pattern after reset.)
2. If the register is ok then continue with next step else give an error and stop testing.
If error,

display: 9C Er19

STEP 10 SLAVE processor (68HC05)

This test checks the communication with the slave processor.

Additionally it displays the slave and cd processor release numbers. If the communication with the cd processor via SPI does not function, the cd release number will give a 0.0.

Address range: Slave base address + 6 (See table).

STEP 10A : WRITE REQUEST BYTE TO THE SLAVE

display: 10A

In this step a \$F0 (request) is written to the slave.

STEP 10B : READ ACKNOWLEDGE FROM THE SLAVE

display: 10B

In this step the following actions take place:

1. wait about 2 sec to give the slave the time to acknowledge.
2. read the acknowledge.
3. if the acknowledge is \$F0 then continue else give an error and stop testing.
If error,

display: 10B Er20

STEP 10C : READ AND DISPLAY SLAVE RELEASE NUMBER

display: 10C

In this step the following actions take place:

1. read the next byte from the slave
2. if the byte «gd» \$00 then continue with step 3 else give an error and stop testing.
If error,

display: 10C Er21

3. wait until a key is pressed.
4. continue with next step

STEP 10D : READ AND DISPLAY CD RELEASE NUMBER

display: 10D

In this step the following actions take place:

1. read the next byte from the slave
2. if the byte $\lt \gt$ \$00 then continue with step 3 else give an error and stop testing
If error,

display: 10D Er22

3. wait until a key is pressed.
4. read the next byte: this is a dummy read.

STEP	DESCRIPTION
0a	VSC master initialization
0b	VSC slave initialization
1a	ROM10 release number
1c	ROM10 checksum check
5	NVRAM test with rom data as data
6af	DRAM fill bank0&bank1 with address as data
6ar	DRAM read and compare data
6bf	DRAM fill bank0&bank1 with inverted add. as data
6br	DRAM read and compare data
7af	DRAM fill bank0 with address as data
7ar	DRAM read and compare
7bf	DRAM fill bank0 with inverted address as data
7br	DRAM read and compare data
8af	DRAM fill bank1 with address as data
8ar	DRAM read and compare
8bf	DRAM fill bank1 with inverted address as data
8br	DRAM read and compare data
9a	CDIC RAM test with address as data
9b	CDIC RAM test with inverted address as data
9c	CDIC register test
10a	SLAVE test: write request to slave
10b	SLAVE test: read echo from slave
10c	SLAVE test: read SLAVE release number from slave
10d	SLAVE test: read CD release number from slave

Table 1: PCB LLTEST steps overview

5.1.6 Terminal low level test

If a VT100 or compatible terminal is connected to the 68070's UART of the CDI player one is able to execute the terminal low level test. Due to the fact that almost every test is self explanatory only the major steps are described below. In this test it is possible to skip every major step.

Display lltest header and release number

STEP 0: VSC

Both master and slave vsc are low level initialized sequentially. This is done the same as in the pcb low level test.

STEP 0: Writing to a user definable ram address

This test writes the powers of 2 to a (word) address. The result is read again and will be displayed. The address can be selected by the user (only word addresses). Pressing 'ESC' stops the test.

If one tries to write to unused space in the memory map, the program will NOT generate an error message.

STEP 01: ROM

For the ROM the following information is displayed and checked:

- Display the identification code for this ROM (ROM ID)
- Display the release number of this ROM
- Display the checksum of this ROM. The upper word of the checksum displayed is always '0000'.
If the checksum is not ok then a specific error will be displayed. This error is the same as in the pcb low level test.

STEP 05: NVRAM

For the NVRAM test three different tests can be selected:

- The first is a non destructive nvram test as in the pcb low level test.
- The second test is a destructive nvram test with ROM data as test data.
- The third test is also a destructive test with the address as data.
- The third test has also some hidden functions. Pressing:
w: writes continu the address as data to the nvram.
r: reads continu the complete nvram (no display).
d: displays the contents of 421 succeeding ram locations. The start address is given by the user.
ESC stops these functions.

Remark: The error message is different from the pcb lltest.

See error table for more information.

Address range: Full nvram address range (see table of memory map)

STEP 06-08: DRAM

The dram test is always a destructive test. The test is performed for both ram bank0 and bank1 as one large memory followed by a test for each bank separately. The following actions take place in the dram test:

1. fill the memory with the long word address as data.
2. read the memory contents and compare with the address.
3. if the long word read is ok then continue else give error message and stop testing.
4. write the inverted long word address as data to memory.
5. read the memory contents and compare with the inverted address.
6. if the long word read is ok then continue else give error message and stop testing.

This test has also some hidden functions. Pressing:

w: writes continu the long address as data to the dram.
r: reads continu the dram (no display).
d: displays the contents of 421 succeeding ram locations. The start address is given by the user.
ESC stops these functions.

Remark: the error message is different from the pcb lltest.

See error table for more information.

Address range: full address range (see product spec)

Bank0 = lower RAM bank
Bank1 = upper RAM bank

STEP 09: CDIC

cdic register2:
CDIC base address + \$3FFA ; register2 contents after reset: \$D7FE

See table of memory map for base address.

The cdic test consists out of three main parts:

- 1 test cdic ram with long word address as pattern
- 2 test cdic ram with inverted long word address as pattern
- 3 display cdic register and compare

If in one of these tests an error occurs the test will be stopped and the error displayed.

This test has also some hidden functions. Pressing:
 w: writes continu the long address as data to the cdic.
 r: reads continu the complete cdic (no display).
 d: displays the contents of 421 succeeding ram locations.
 The start address is given by the user.
 ESC stops these functions.

Address range:
 CDIC base address + \$1400 to CDIC base address + \$3C80.

- STEP 10: SLAVE processor (68HC05)
 This lltest for the slave performs following actions:
- 1 Write \$F0 to the slave processor.
 - 2 Read byte from same address, the slave should respond with \$F0.
 - 3 If data is not \$F0 then stop testing and display error code else continue with next action.
 - 4 Read the next byte: this byte is the release number of the slave processor firmware. Display the release number. If the release number is \$00 then an error will be displayed.
 - 5 Read the next byte: this byte is the release number of the CD processor firmware. Display the release number. If the release number is \$00 then an error will be displayed.
 - 6 Read the next byte: this is a dummy read.

Address range: Slave base address + what is read in 6.

See table of memory map for base address.

STEP 11: CLOCK CALIBRATION
 This step is not really a test. it is a software tool that can be used to trim the clock&calendar chip so that it runs within 1 minute acc. per month. If calibration is not needed, this step should be executed since a frequency counter is needed to complete this test successfully. If this test is entered accidentally, just switch off the power and restart the lltest.
 The clock calibration should be performed with an external frequency counter.

- Connect the probe of the counter to pin21 of IC7205 the signalis called CSCDICN.
- Start the test with the gate time of the frequency counter set to minimum 5 sec.
- The counter display should now show a frequency near to 512 Hz.
 If not, the chek if everything is set and connected properly.
 (range : 511,96724 to 512,03276)
- Press a key on the terminal to stop the measurement.
- Now fill in the measured value of the frequency. The lltest software will now calculate the proper value to be filled into the calibration register of the clock&calendar IC.
 The value of the frequency at pin21 of IC7205 will not be changed or influenced.
- The calibration is done now.

5.1.7 Error codes

When during a test an error occurs the user should be aware of following conventions:
 - For the pcb low level test the error is displayed on the outermost righthand side of the display.

Example: 1 Er11

An survey for all error codes is given in table 2.

- For the terminal low level test the error is displayed on the outermost lefthand side of the terminal. In some cases (memory tests) the error code is replaced by a more meaningful error output.

Example: ADDRESS DATA READ EXPECTED
 ERROR:00080000 F0080000 00080000 RETURN to continue,ESC to STOP

Meaning: (assuming long word data is used); On address \$80000 the data was \$F0080000 and not \$80000 as it should be. If the RETURN button is pressed, the next address will be read and checked. With this output it will be easier to debug the MMC board

- When an error has occurred the program will wait for a user intervention with following question: RESTART the test Yes or No?
 If the answer was 'Y' then the lltest software is executed again from the beginning.
 If the answer was 'N' then the next test is executed as if nothing happened.

ERROR	DESCRIPTION	DISPLAY
05	ROM checksum error	Er05
09	NVRAM error	Er09
10	NVRAM error (for inverted data)	Er10
11	DRAM error (bank0 & bank1)	Er11
12	DRAM error (bank0 & bank1, inverted data)	Er12
13	DRAM bank0 error	Er13
14	DRAM bank0 error (inverted data)	Er14
15	DRAM bank1 error	Er15
16	DRAM bank1 error (inverted data)	Er16
17	CDIC RAM error	Er17
18	CDIC RAM error (inverted data)	Er18
19	CDIC register error	Er19
20	SLAVE error (wrong echo from slave)	Er20
21	Invalid release number from slave	Er21
22	Invalid release number from cd proc	Er22

Table 2. Error codes overview

5.1.8 Release number, position and checksum storage

The release number, ID and checksum are always stored in the CDI ROM. Step 1 of the pcb lltest as well as the terminal lltest uses all this information to check if the ROM is ok.

Where are these bytes stored in the ROM's, where in the memory?
 (ROM address range for the 4Mb: \$00000-\$7FBFF)
 (MMC address range for the 1Mb: \$180000-\$1FFBFF)

- ROM address \$7FBFF = LSByte of the checksum
 \$7FBFE = MSByte of the checksum
 \$7FBFD = Release number of this ROM (BCD coded)
 \$7FBFC = Player ID (BCD coded)
 MMC address \$1FFBFF = LSByte of the checksum of the ROM
 \$1FFBFE = MSByte of the checksum of the ROM
 \$1FFBFD = Release number of the ROM (BCD coded)
 \$1FFBFC = Player ID (BCD coded)

Remark: The total ROM space is 512k minus 1k. This 1k can never be accessed in the MMC address space. It is used for the VSC's registers and chip selects.

5.1.9 How is the checksum calculated?

The checksum is calculated for every ROM separately. The checksum is the algebraic sum of all bytes in that ROM except the 2 bytes where the checksum is written. Only the LSWord of the sum is used. To calculate the real checksum of the ROM just add these 2 bytes to the LSWord of the sum.
 The last 1024 bytes are always assumed to be all \$FF.

ROM checksum = sum of all bytes of the address range \$180000 to \$1FFBFD + \$FC00
 ROM checksum displayed in STEP 1 = ROM checksum + (LSB + MSB) of this checksum.
 This is also equal to the checksum of the complete ROM.

5.2 THE SERVICE SHELL

Introduction.

For service purposes the CD-I set has built-in software modules. These modules can be activated via the service shell by menu.

- The modules are for the testing of :
- Video circuitry, by means of a colorbar testpatern
 - CDM and servo circuitry
 - Input / Output ports
 - Audio circuitry

Testing the CDM, servo and audio cicuitry in the service shell is only possible with a CD-DA disc.

5.2.1 Starting the service shell

The service shell can be started by connecting the RXD and TXD lines of port 1 (pin2 and pin3) during start up (insert testplug before power on or reset).

5.2.2 Layout info

SELECTABLE/NON SELECTABLE ITEMS

Each menu of the service shell consist of a number of boxes and text strings. Some of these boxes can be selected by moving the screen cursor above the box and clicking on one of the joystick buttons. Only the colored boxes can be selected. Clicking on one of the other boxes will have no effect.

(ERROR) MESSAGES ON THE SCREEN

The service shell will provide information and errors in a box at the top of the screen. To remove such a message and continue with the test a button must be clicked on the remote control joystick.

MENU STRUCTURE

When the service shell is started, the main menu appears with a number of boxes on it. Selecting some boxes will result in a submenu being displayed, other boxes may result in immediate action. Selecting the EXIT box will stop the service shell and restart the player. Selecting EXIT in a submenu will return you to the previous menu.

5.2.3 Subject dependent information

MAIN MENU

The main menu contains four test item boxes and the EXIT box. Selecting TEST IMAGE will give immediate action, the other three test items will display a submenu.

CD TEST

This menu has two information boxes at the top of the screen. Below it are three test items for the CD player and below these are three buttons that can be selected only during the CD drive test. When the menu is first entered, only the three test item boxes can be selected. Subjects of the CD test are the cd drive itself, the X bus and a test on Digital Out.

When this menu is selected in the main menu, the communication channel with the CD processor will be checked first. A message will be displayed giving the result of this check (either O.K. or No response). After pressing one of the buttons (to remove the message) the cd menu will be displayed.

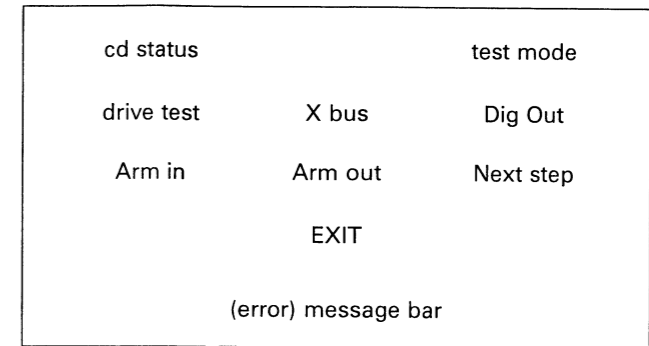


fig 3.2 CD test menu

The X bus test will result in immediate action. It checks the communication channel between the CDIC and CD processor that is normally used to send commands (seek, read etc) to the CD processor. The result is either O.K or No response.

The Dig. Out test will also give immediate action. It's purpose is to check wether the CDIC receives a Digital Out signal or not. The result of this test is O.K. or No Digital Out. The CD drive test uses a different menu and will therefore be described in a separate paragraph.

CD DRIVE TEST

The CD drive test will perform the service loop as implemented in the Philips CD audio players. A disc is needed for this test. Results of this test will be displayed on the screen instead of a display. When the cd drive test is selected, the same screen will appear, but with other buttons highlighted. You cannot select the X bus and Dig Out test anymore. Selecting the EXIT button will return you to the cd menu. (X bus and Dig Out button highlighted again). The drive test consist of the following steps:

Mode 0

Software release number of the CD micro processor is displayed in the button at the left top of the screen (cd status button). Mode 0 is displayed in the button at the right top of the screen (mode button). During the cd drive test this button will display the current mode.
 In mode 0, the ARM IN and ARM OUT buttons can be selected to move the cd lense inwards and outwards. Selecting NEXT STEP will bring the player in mode 1.

Mode 1
 In mode 1 ages to do FOCUS wi message l the cd driv take a whi turn to mc Selecting l

Mode 2
 The turnta HF, movin: disc down If an error Selecting l mode 3.

Mode 3
 You can se jump insid jumping w If an error NEXT STE ing mode.

Normal pl: The player processor cannot ret ting the pl

ERROR MI display: A

xx = 2 :
 xx = 3 :
 xx = 5 :
 xx = 6 :
 xx = 7 :
 xx = 8 :

xx = 30 :
 xx = 31 :
 xx = 32 :
 xx = 33 :
 xx = 34 :
 xx = 37 :

DUART TE This test is

APU/KEY This is a c via this m can be tes tenuation (to increm current att MONO/ST tenuation in MONO attenuatio audio disc routine wi When a ke on the rigl pressed. T

ROM address \$7FBFF = LSByte of the checksum
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 \$7FBFD = Release number of this ROM (BCD coded)
 \$7FBFC = Player ID (BCD coded)
 MMC address \$1FFBFF = LSByte of the checksum of the ROM
 \$1FFBFE = MSByte of the checksum of the ROM
 \$1FFBFD = Release number of the ROM (BCD coded)
 \$1FFBFC = Player ID (BCD coded)

Remark: The total ROM space is 512k minus 1k. This 1k can never be accessed in the MMC address space. It is used for the VSC's registers and chip selects.

5.1.9 How is the checksum calculated?

The checksum is calculated for every ROM separately. The checksum is the algebraic sum of all bytes in that ROM except the 2 bytes where the checksum is written. Only the LSWord of the sum is used. To calculate the real checksum of the ROM just add these 2 bytes to the LSWord of the sum.

The last 1024 bytes are always assumed to be all \$FF.

ROM checksum = sum of all bytes of the address range \$180000 to \$1FFBFD + \$FC00
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The service shell will provide information and errors in a box at the top of the screen. To remove such a message and continue with the test a button must be clicked on the remote control joystick.

MENU STRUCTURE

When the service shell is started, the main menu appears with a number of boxes on it. Selecting some boxes will result in a submenu being displayed, other boxes may result in immediate action. Selecting the EXIT box will stop the service shell and restart the player. Selecting EXIT in a submenu will return you to the previous menu.

5.2.3 Subject dependent information

MAIN MENU

The main menu contains four test item boxes and the EXIT box. Selecting TEST IMAGE will give immediate action, the other three test items will display a submenu.

CD TEST

This menu has two information boxes at the top of the screen. Below it are three test items for the CD player and below these are three buttons that can be selected only during the CD drive test. When the menu is first entered, only the three test item boxes can be selected. Subjects of the CD test are the cd drive itself, the X bus and a test on Digital Out.

When this menu is selected in the main menu, the communication channel with the CD processor will be checked first. A message will be displayed giving the result of this check (either O.K. or No response). After pressing one of the buttons (to remove the message) the cd menu will be displayed.

cd status		test mode
drive test	X bus	Dig Out
Arm in	Arm out	Next step
	EXIT	
(error) message bar		

fig 3.2 CD test menu

The X bus test will result in immediate action. It checks the communication channel between the CDIC and CD processor that is normally used to send commands (seek, read etc) to the CD processor. The result is either O.K or No response.

The Dig. Out test will also give immediate action. It's purpose is to check whether the CDIC receives a Digital Out signal or not. The result of this test is O.K. or No Digital Out. The CD drive test uses a different menu and will therefore be described in a separate paragraph.

CD DRIVE TEST

The CD drive test will perform the service loop as implemented in the Philips CD audio players. A disc is needed for this test. Results of this test will be displayed on the screen instead of a display. When the cd drive test is selected, the same screen will appear, but with other buttons highlighted. You cannot select the X bus and Dig Out test anymore. Selecting the EXIT button will return you to the cd menu. (X bus and Dig Out button highlighted again). The drive test consist of the following steps:

Mode 0

Software release number of the CD micro processor is displayed in the button at the left top of the screen (cd status button). Mode 0 is displayed in the button at the right top of the screen (mode button). During the cd drive test this button will display the current mode.

In mode 0, the ARM IN and ARM OUT buttons can be selected to move the cd lense inwards and outwards. Selecting NEXT STEP will bring the player in mode 1.

Mode 1

In mode 1 the cd driveprocessor will try to focus. If it manages to do so (a disc must be present!), the message IN FOCUS will appear in the status button. Otherwise, the message NO FOCUS will appear in the status button after the cd driveprocessor has tried to focus 16 times (this may take a while). In that case (no focus found) the test will return to mode 0.

Selecting NEXT STEP will bring the player in mode 2.

Mode 2

The turntablemotor is rotating and controlled by the rough HF, moving the cd lense outside (by hand) will slow the disc down.

If an error occurs, the test will return to mode 0.

Selecting NEXT STEP in mode 2 will bring the player in mode 3.

Mode 3

You can select ARM IN and ARM OUT to make the cd lense jump inside or outside (small jumps). The laser will keep jumping while a button is pressed on the remote control. If an error occurs, the test will return to mode 0. NEXT STEP in mode 3 will bring the player in normal playing mode.

Normal playing mode

The player shell will be started and errors sent by the cd processor will be displayed in a box on the screen. You cannot return to the service shell otherwise than by resetting the player.

ERROR MESSAGES

display: A5 xx0000

- xx = 2 : focus error
- xx = 3 : radial error
- xx = 5 : off error (TL stays low for 50 msec.)
- xx = 6 : jump error
- xx = 7 : subcode error, no valid subcode in 3 sec.
- xx = 8 : TOC error: out of lead-in area while reading the TOC
- xx = 30 : too many grooves to jump
- xx = 31 : search time out
- xx = 32 : bin. search error
- xx = 33 : search index error
- xx = 34 : search time error
- xx = 37 : selection error

DUART TEST

This test is not relevant for the CDI205

APU/KEY TEST

This is a combined menu, the attenuation can be changed via this menu and the keys on remote control and player can be tested with it. There are three buttons for every attenuation path on the screen. Two of them can be selected (to increment/decrement) and one is used to display the current attenuation value for the path. There is also a MONO/STEREO button on the screen. In STEREO, two attenuation paths are disabled (left to right and right to left), in MONO all attenuation paths are enabled. Maximum attenuation is reached at the value 47 (no sound). A CD audio disc is needed for the attenuation test. The test routine will start playing the disc at initialization. When a key is pressed, a text will appear on the key button on the right side of the screen describing the button pressed. The text will disappear when the key is released.

LEFT/LEFT - 00 +	RIGHT/RIGHT - 00 +
LEFT/RIGHT - 00 +	RIGHT/LEFT - 00 +
STEREO/MONO STEREO	LAST KEY EXIT
(error) message bar	

fig 3.4 APU test menu

VIDEO TEST IMAGE

A colorbar will be displayed on the screen. Pressing a button after the screen has been filled completely will return you to the main menu. There are no error messages for this test.

What could be wrong if...

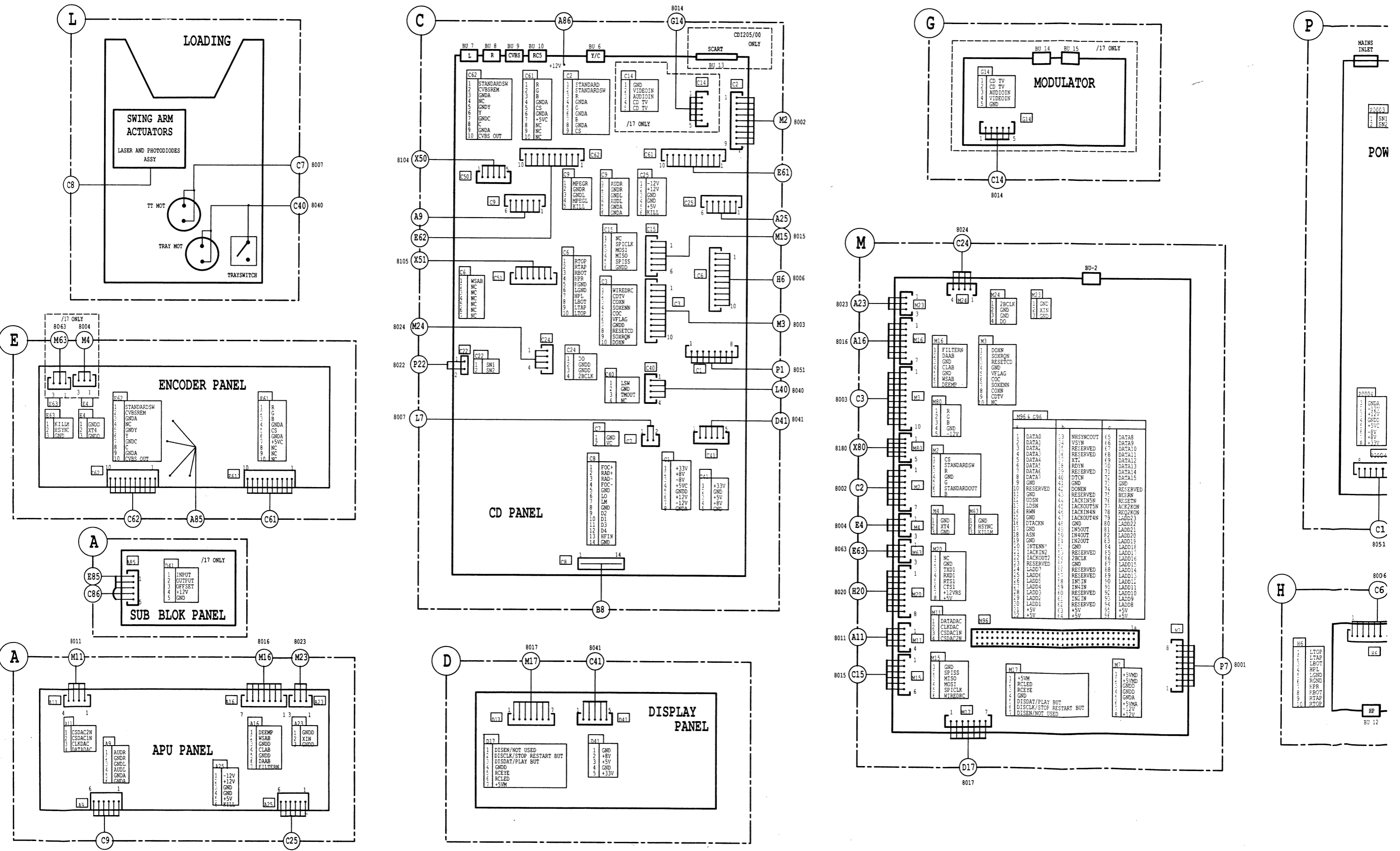
This paragraph will describe the meaning of the error messages given by the service shell and contains suggestions about possible errors. This paragraph must be updated with new information from testing and debugging players.

Service shell cannot be started with the testplug. Connections between port 1 and slave may be bad. Testplug could be wrong. Maybe the slave processor is defect. If the playershell cannot be started either, try the low level test first.

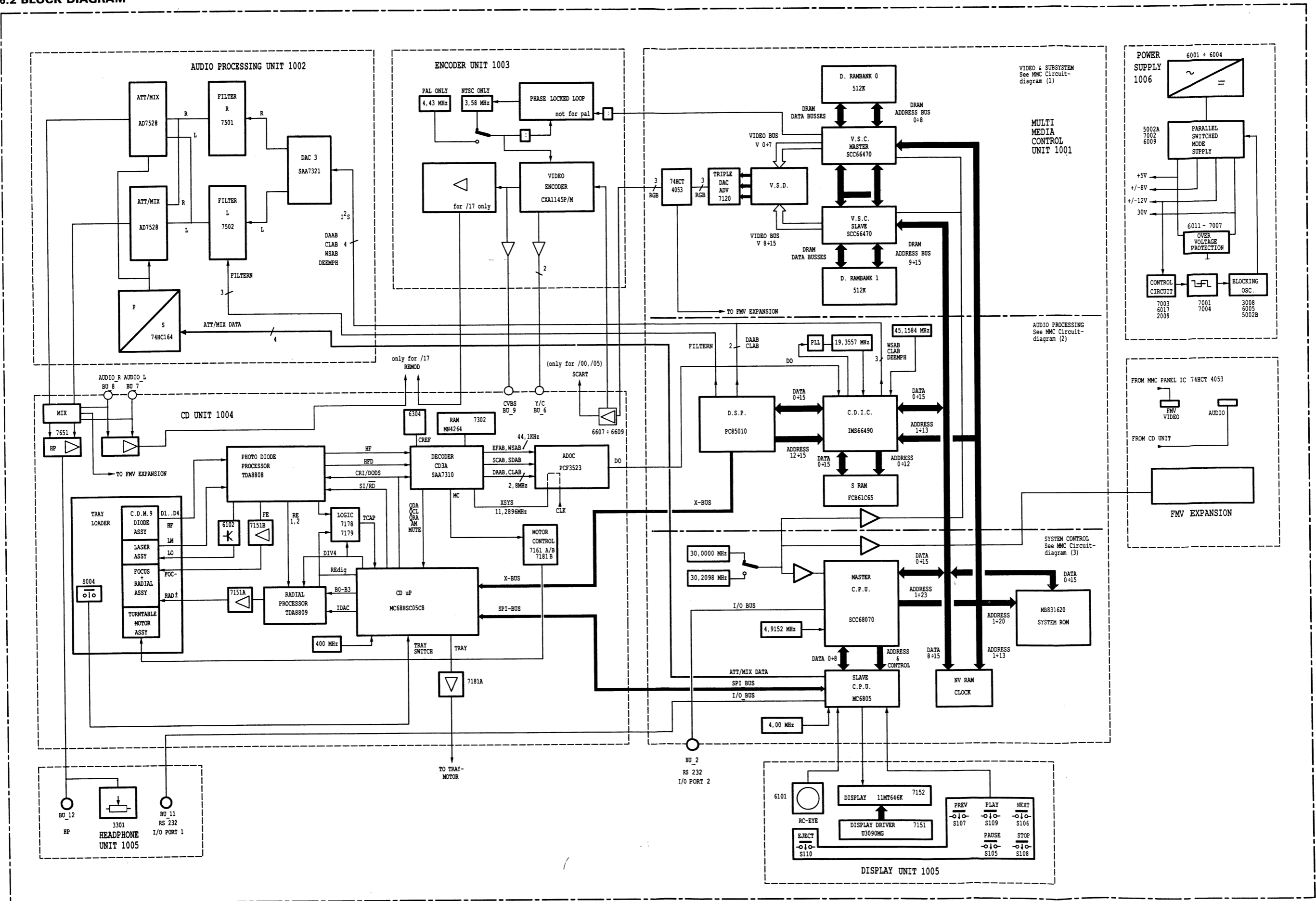
The key test will display the text ERROR if an unknown key code is received.

Disconnecting the clock from MMC to CD processor will make the CD player turn as fast as it can.

6.1 WIRING DIAGRAM



6.2 BLOCK DIAGRAM



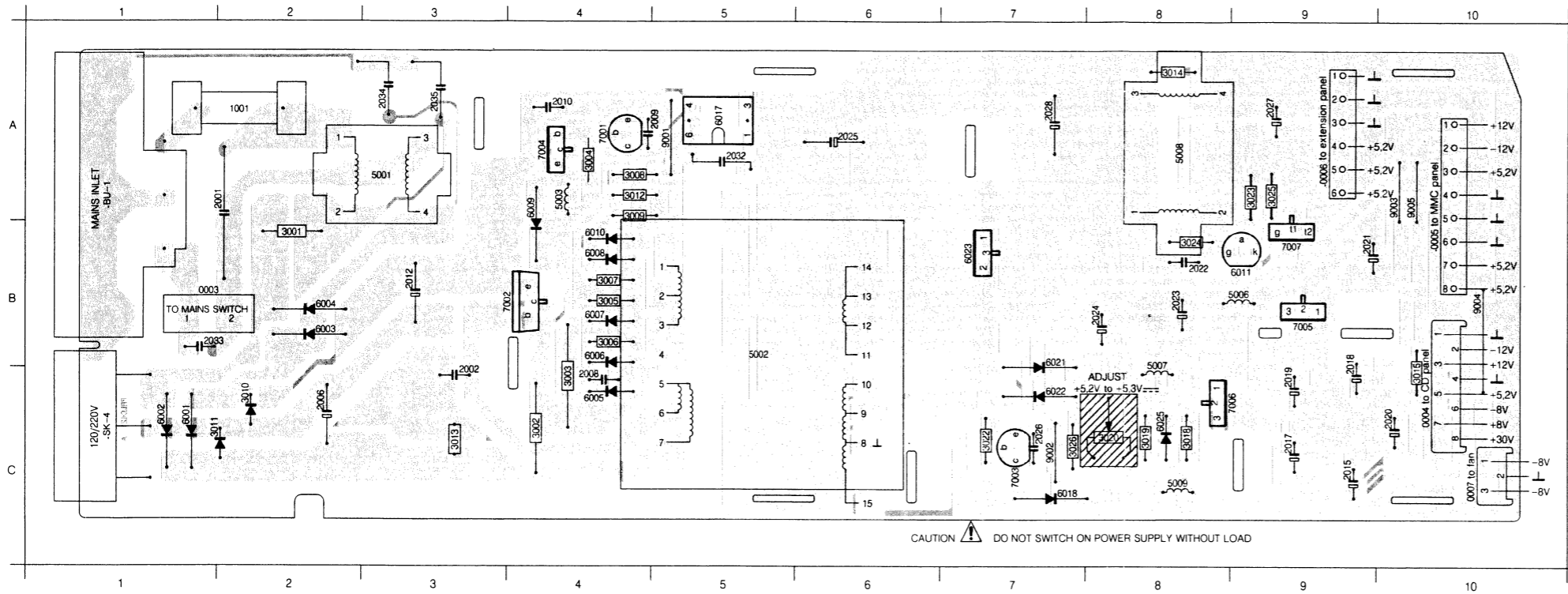
6.2.1 Alphabetical signal listing

A,B,C +	: >> control signals for brushless DC-motor	CSYN	: COMPOSITE SYNCHRONIZATION input from the VSC's (active low)	IACKOUT22	: >>	RBOT	: for HPR volume control
A,B,C -	: >>	CTS1..4	: CLEAR TO SEND (active low) it indicates that the remote receiving device is ready	IACKOUT23	: >>	RCEYE	: REMOTE CONTROL EYE
ACK2N	: DMA REQUEST ACKNOWLEDGE (active low) (of channel 2)	CTS 2	: >>	IACKOUT42	: >>	RCLED	: REMOTE CONTROL LED
ACM	: output AC-motor	CVBS	: CVBS output	IACKOUT52	: >>	RD	: READY signal, starting up procedure finished
ADEN	: (=ADENA) ADDRESS ENABLE NOT. When low, the address ADENA coming from the bus (68070) will be put through to CDIC	D1..4	: fotodiode currents	IDAC	: 1/2 bit DAC	RDYN	: READY (active low) of the DMA channel
AM	: ADDITIONAL MUTE	DAAB	: (DAAB2) serial data output of the X-bus I ² S standard	IDTACKN	: data transfer acknowledge from 68070	REDIG	: RADIAL ERROR DIGITAL
ASN	: ADDRESS STROBE (active low, tristate) indicates when an address is valid on the bus for the system	DATA 0..15	: DATA LINES	IFDN2	: main channel word-flag to the DSP	RESETCD	: when low resetsequence starts
AUDL	: >> AUDIO LEFT	DATADAC	: Data which will be send to the DAC('S) for volume adjustment	INTENN	: >> when low, no extensions use the interrupts, when high interrupt devices are daisy chained	RESETINN	: when low VSC is in reset
AUDIOL	: >>	DDTACK	: DATA TRANSFER ACKNOWLEDGE to the 68070 bus	INTENN2	: >>	RESETN	: this is the reset for all other ic's
AUDR	: >> AUDIO RIGHT	DEEMP	: DEEMPHASIS	INTENN3	: >>	REQ2N	: DMA-request of the second channel
AUDIOR	: >>	DIG OUT	: DIGITAL OUTPUT	INTENN4	: >>	RSTOUT	: RESET OUT of the slave processor when high resetsequence starts
AVN	: AUTOVECTORED INTERRUPTS (active low), can be used by an extension	DIRN	: DIRECTION CONTROL. Indicates the direction of data transfer through the transceivers	IN2IN	: (=IN2OUT) >>	RTAP	: >> for HPR volume control
B0..3	: input control bits for off-, catch-, play status and DAC output current for radial motor	DO	: DIGITAL OUTPUT	IN4IN	: (=IN4UT) >> Decoder interrupt priority inputs	RTOP	: >>
B,G,R,	: Output colours of the VSR	DODS	: DROP-OUT DETECTOR SUPPRESSION	IN5IN	: (=IN5OUT) >> (active low) IN2IN has the lower	RTSUART	: REQUEST TO SEND from the slave processor to the UART of the 68070 processor
BERRN	: >> BUS ERROR (active low, open drain)	DONEN	: DONE (active low, open drain), operates in the DMA-mode	IN2OUT	: >> and IN5IN has the higher priority	RTS1..4	: >> REQUEST TO SEND (active low)
BERR	: >>	DOXN	: serial data output of the X-bus	IN4OUT	: >> IN2IN = SLAVEPROCESSOR (6805), IN4IN =	RTS 1..2	: >>
BLANI	: (=BLAN1M) BLANKING OUTPUT (active low, tristate) of the VSC	DPSRWN	: Read (high) or write (low) from or to the Digital Signal Processor	IN5OUT	: >> CDIC (IMS66490), IN5IN = DUART (68681)	RWN	: READ - WRITE (low is write) signal
CADDYIN	: high when reading data	DSN2N	: DATA STROBE (active low) of the DSP	IN4OUT2	: >>	RWN2	: READ - WRITE (low is write) signal from CDIC to the DSP
CADDYSWITCH	: control signal for position tray	DTACKN	: DATA TRANSFER ACKNOWLEDGE asserted by a peripheral	IN5OUT2	: >>	RWRAM	: READ - WRITE signal from the CDIC to the S-RAM'S
CASN	: COLUMN ADDRESS STROBE (active low)	DTACKSLAVEN	: DATA TRANSFER ACKNOWLEDGE of the SLAVE processor (68HC05)	IN2OUT3	: >>	RXD1..4	: >> RECIEVE DATA RXD is data input
CBA, CBAA	: 68070 bus transiever latch (rising edge)	DTCN	: DATA TRANSFER COMPLETE (active low, open drain) operates in the DMA-mode	KILL	: to mute audio outputs by power on and off	RXD 1..2	: >>
CDICDACKN	: (=ACK1N) DMA REQUEST ACKNOWLEDGE (active low)	DUARTCSN	: DUART CHIP SELECT, when low businfo is coming from or going to the DUART	LA1	: >> control signals for brushless DC-motor	SI	: on - off control for laser supply and focus circuit
CDICREQN	: (=REQ1N) DMA REQUEST (active low)	EFAB	: ERROR FLAG	LB1	: >>	SLMA0..8	: VSC-slave memory address bus to the DRAM'S
CDTV	: to change by remote control between TV or CDI (only used by CDI 2XX)	FILTERN	: filter select when high: level C, when low: level A	LC1	: >>	SLMD0..15	: VSC-slave memory data bus to the DRAM'S
CLAB	: (=CLAB2) bitclock for the SAA 7220 chip	FOC-	: >> focus out to CDM 9	LADD1..23	: ADDRESS-BUS (active high, tristate) for direct addressing of 16 Mbyte of memory	SOXENN	: SERIAL OUTPUT ENABLE FOR THE X-BUS (enabled when low)
CLK	: CLOCK (11,2896 Mc)	FOC+	: >>	LBOT	: for HPL volume control	SOXRQN	: SERIAL OUTPUT REQUEST FOR THE X-BUS (when low)
CLKDAC	: CLOCK DAC, the clock used to send serial data to the volume adjustment	GN	: >>	LDSN	: LOWER DATA STROBE of the bus	SOYENN2	: SERIAL OUTPUT ENABLE FOR THE Y-BUS (when low)
CLK1	: the clock on which the DSP operates (7,5264 Mc)	GNA	: >> When low: the outputs and inputs of the transceivers (646) are enabled	LM	: LASER MONITOR diode input	SPICLK	: SERIAL PERIPHERAL INTERFACE CLOCK
CRI	: COUNTER RESET INHIBIT (low during a real trackloss or during execution of a jump command)	GNB	: >>	LO	: LASER amplifier current OUTPUT	SPISS	: SERIAL PERIPHERAL INTERFACE SLAVE SELECT
COC	: COMMAND COMPLETED signal	HALTN	: active low, open drain, bidirectional. If low together with the resetn it causes the 68070 to enter the reset state.	LRDN	: when low select, the ROM'S or NVRAM read the lower data byte	STANDARD	: software choice between PAL and NTSC
COXN	: serial output clock for the X-bus	HFin	: HF current input	LTAP	: >> for HPL volume control	STANDARDSW	: hardware choice between PAL and NTSC
CPUASN	: the address strobe of the 68070 microprocessor	HPL	: HEADPHONE LEFT	LTOP	: >>	SSM	: START/STOP MOTOR
CPULDSN	: the lower data strobe of the 68070 microprocessor	HPR	: HEADPHONE RIGHT	LVID0IN..	: >>	SWAB	: SUBCODING WORD CLOCK INPUT
CPUUDSN	: the upper data strobe of the 68070 microprocessor	HSYN	: (active low) horizontal synchronisation input from the VSC	..LVID7IN	: >> 8 bit pixel-bus for channel 2 (VSC-SLAVE)	SYSCLK	: >> SYSTEM CLOCK
CS	: CHIP SELECT	HSYNOUT	: (active low) horizontal synchronisation output for monitor or tv	..LVID7OUT	: >>	SYSCLK1	: >>
CSCDICN	: CHIP SELECT CDIC (active low) bus information is intended for or coming from CDIC	..HVID 7 IN	: >> 8 bit pixel bus for channel 1	MC	: MOTOR CONTROL signal	TCAP	: input capture feature for the on-chip timer
CSDAC1N	: (=CSDAC2N) (if selected, low) it means that data will be adjusted on that channel	HVID 0 OUT..	: >> (VSC-master)	MISO	: MASTER IN SLAVE OUT	TCMP	: output for the output compare feature of the on chip timer
CSNVRAMN	: CHIP SELECT NVRAM (active low) bus information is intended for or coming from the NVRAM	HVID 7 OUT	: >>	MOSI	: MASTER OUT SLAVE IN	TMOUT	: TRAY MOTOR OUT
CSROMN	: >>	IACKIN2N	: >>	MSMA0..8	: ADDRESS BUS between the DRAM'S of the VSC' MASTER and the VSC MASTER	TXD1..4	: >> TRANSMIT DATA TXD is data output
CSROM1N	: CHIP SELECT ROM (active low) bus information is coming from the ROM'S	IACKIN4N	: >> Decoded interrupt acknowledge (active low).	MSMD0..15	: DATA BUS between the DRAM'S of the VSC' MASTER and the VSC MASTER	TXD 1..2	: >>
CSROM2N	: >>	IACKIN5N	: >> Asserted during an interrupt acknowledge	NRESET	: when low the video synthesizer (VSR) is in reset	UDSN	: UPPER DATA STROBE (active when low)
CSSLAVEN	: CHIP SELECT SLAVES (active low)	IACKOUT2N	: >> sequence to indicate to a peripheral that	NVDS	: digital output to control an external switch for TV overlays (active low)	URDN	: READ UPPER DATA BYTE (active when low)
CSON	: (=CSONA) CHIP SELECT (active low) for the 8Kx8 SRAM'S	IACKOUT4N	: >> this interrupt request is being serviced	PCLK1IN	: >> PIXEL CLOCK for channel 1	UWRMN	: READ - WRITE (write when low) UPPER MEMORY DATA FROM DRAM'S FROM VSC-MASTER
CSVSCMSN	: CHIP SELECT VSC MASTER AND SLAVE. When low the coming information is intended for the VSC'S	IACKOUT5N	: >>	PCLK2IN	: >> PIXEL CLOCK for channel 2	UWRN	: WRITE UPPER DATA BYTE (active when low)
		IACKOUT2	: >>	PCLK2OUT	: >>	UWRSN	: READ - WRITE (write when low) UPPER MEMORY DATA FROM DRAM'S FROM VSC-SLAVE
		IACKOUT4	: >>	PLOIN1	: input clock for CDIC (22,5792 Mc)	VC	: output DC-motor (VOLTAGE CONTROL)
		IACKOUT5	: >>	PLOIN2	: input clock for CDIC (19,3536 Mc)	V-FLAG	: output to the DSP
				QCL	: Q-channel CLOCK	VSCM-INTN	: when low, interrupt from VSC master to 68070 processor
				QDA	: Q-channel DATA	VSCS-INTN	: when low, interrupt from VSC slave to 68070 processor
				QRA	: Q-channel REQUEST INPUT/ ACKNOWLEDGE OUTPUT	VSYN	: (active when low) VERTICAL SYNCHRONISATION INPUT from the VSC
				Q22	: output to PLL (22,5792 Mc) divided by 14		
				Q21	: output to PLL (19,3536 Mc) divided by 12		
				RAD+	: >> RADIAL OUT to CDM 9		
				RAD-	: >>		
				RASN	: ROW ADDRESS STROBE (active low)		

WRPN1IN..2 : >> control input for channel 1 or 2
 (active low)
 WRPN1OUT.2 : >>
 WSAB : >> WORD SELECT FOR AB CHIP
 WSAB2 : >>
 XIN : >> 11,2896/9,6768/4,8384 symmetrical
 clock
 XIN2 : >>
 X-TAL2 : the same as the system clock,coming
 out of the VSC'S
 XT2 : the system clock devided by two
 XT4 : >> the system clock devided by four
 XT4IN : >>
 0AD..12AD : >> ADDRESS BUS,between CDIC-
 SRAM'S and SYSTEM ADDRESS BUS
 BUFFERS

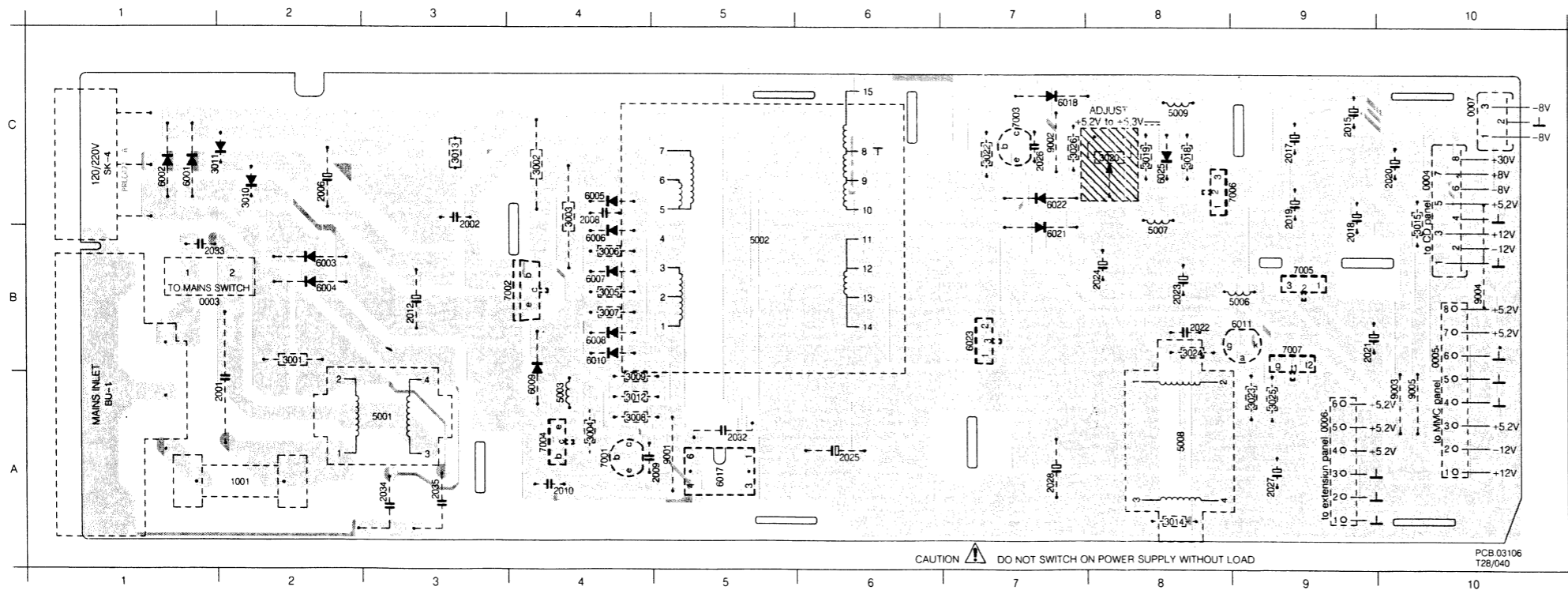
 10ADA..
 ..12ADA : >>
 0D..15D : DATA BUS between CDIC and DSP
 0DA..15DA : DATA BUS between CDIC-SRAM'S and
 SYSTEM DATA BUS TRANCIEVERS
 2BCLK : CLOCK for the 2B-chip
 12A..15A : ADDRESS BUS between CDIC and DSP

6.3.1 POWER SUPPLY PCB, COMPONENT SIDE VIEW



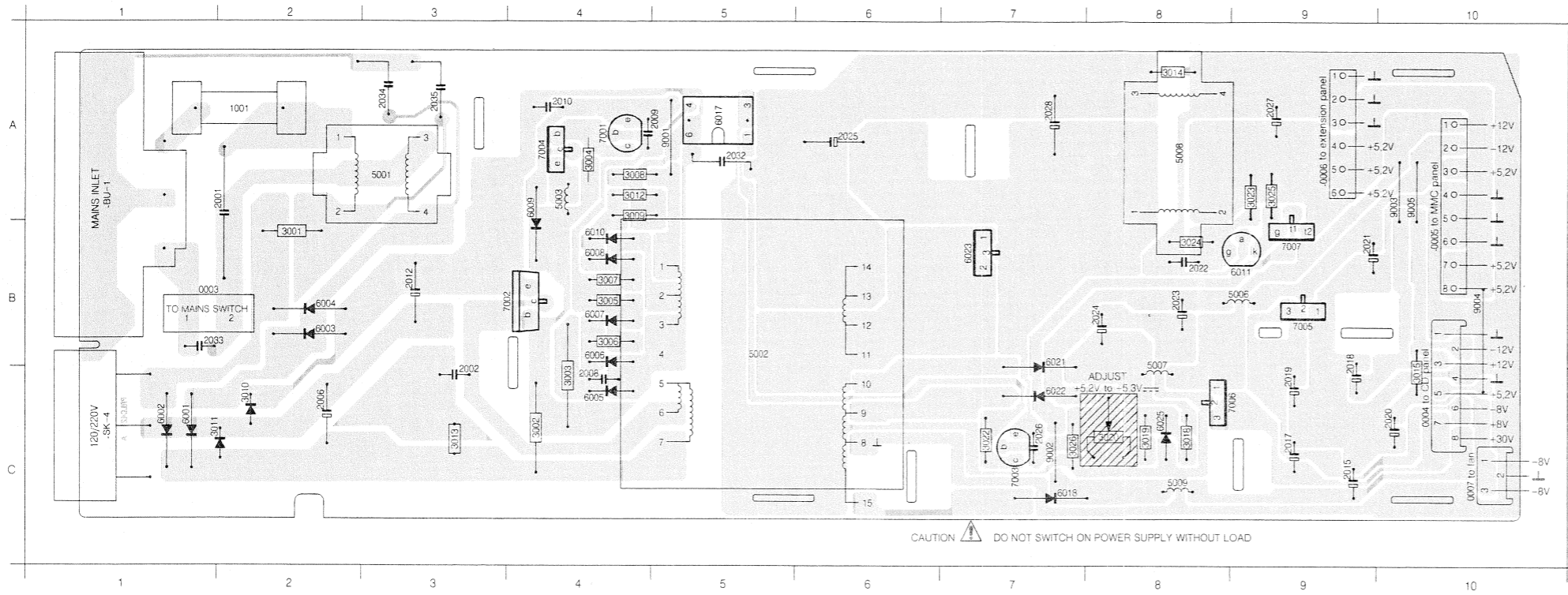
0003 B1	3011 C2	7004 A4
0004 C10	3012 A4	7005 B9
0005 B10	3013 C3	7006 C9
0006 A9	3014 A8	7007 B9
0007 C10	3015 C10	9001 A5
1001 A2	3018 C8	9002 C7
2001 A2	3019 C8	9003 A10
2002 C3	3020 C8	9004 B10
2006 C2	3022 C7	9005 A10
2008 C4	3023 A9	BU-1 A1
2009 A5	3024 B8	SK-4 C1
2010 A4	3025 A9	
2012 B3	5026 C7	
2015 C9	5001 A3	
2017 C9	5002 B5	
2018 C9	5003 A4	
2019 C9	5006 B8	
2020 C10	5007 C8	
2021 B9	5008 A8	
2022 B8	5009 C8	
2023 B8	6001 C1	
2024 B8	6002 C1	
2025 A6	6003 B2	
2026 C7	6004 B2	
2027 A9	6005 C4	
2028 A7	6006 B4	
2032 A5	6007 B4	
2033 B1	6008 B4	
2034 A5	6009 A4	
2035 A3	6010 B4	
3001 B2	6011 B9	
3002 C4	6017 A5	
3003 C4	6018 C7	
3004 A4	6021 B7	
3005 B4	6022 C7	
3006 B4	6023 B7	
3007 B4	6025 C8	
3008 A4	7001 A4	
3009 A4	7002 B4	
3010 C2	7003 C7	

6.3.1 POWER SUPPLY PCB, COPPER TRACK SIDE VIEW



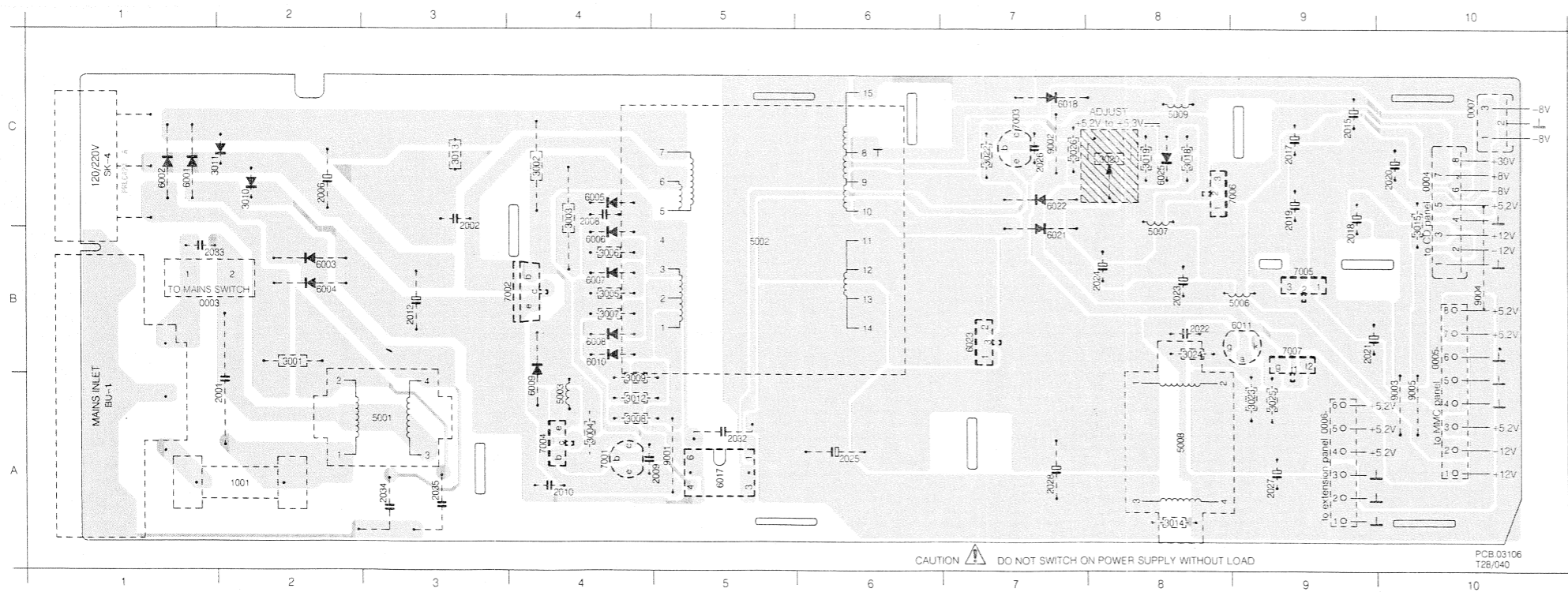
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0004 C10	3012 A4	7005 B9
0005 B10	3013 C3	7006 C9
0006 A9	3014 A8	7007 B9
0007 C10	3015 C10	9001 A5
1001 A2	3018 C8	9002 C7
2001 A2	3019 C8	9003 A10
2002 C3	3020 C8	9004 B10
2006 C2	3022 C7	9005 A10
2008 C4	3023 A9	BU-1 A1
2009 A5	3024 B8	SK-4 C1
2010 A4	3025 A9	
2012 B3	5026 C7	
2015 C9	5001 A3	
2017 C9	5002 B5	
2018 C9	5003 A4	
2019 C9	5006 B8	
2020 C10	5007 C8	
2021 B9	5008 A8	
2022 B8	5009 C8	
2023 B8	6001 C1	
2024 B8	6002 C1	
2025 A6	6003 B2	
2026 C7	6004 B2	
2027 A9	6005 C4	
2028 A7	6006 B4	
2032 A5	6007 B4	
2033 B1	6008 B4	
2034 A5	6009 A4	
2035 A3	6010 B4	
3001 B2	6011 B9	
3002 C4	6017 A5	
3003 C4	6018 C7	
3004 A4	6021 B7	
3005 B4	6022 C7	
3006 B4	6023 B7	
3007 B4	6025 C8	
3008 A4	7001 A4	
3009 A4	7002 B4	
3010 C2	7003 C7	

6.3.1 POWER SUPPLY PCB, COMPONENT SIDE VIEW



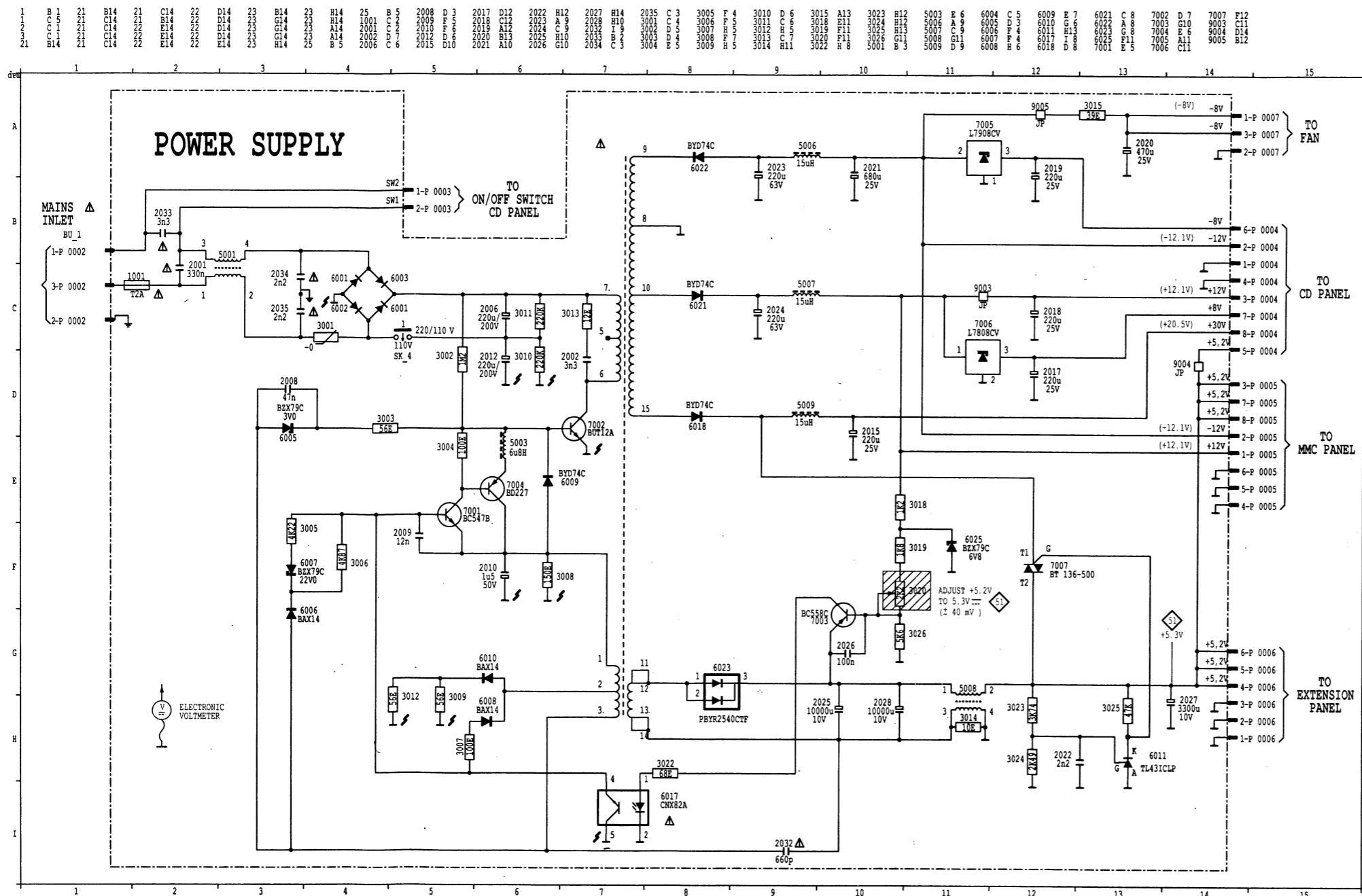
0003 B1	3011 C2	7004 A4
0004 C10	3012 A4	7005 B9
0005 B10	3013 C3	7006 C9
0006 A9	3014 A8	7007 B9
0007 C10	3015 C10	9001 A5
1001 A2	3018 C8	9002 C7
2001 A2	3019 C8	9003 A10
2002 C3	3020 C8	9004 B10
2006 C4	3022 C7	9005 A10
2008 C4	3023 A9	BU-1 A1
2009 A5	3024 B8	SK-4 C1
2010 A4	5025 A9	
2012 B3	5026 C7	
2015 C9	5001 A3	
2017 C9	5002 B5	
2018 C9	5003 A4	
2019 C9	5006 B8	
2020 C10	5007 C8	
2021 B9	5008 A8	
2022 B8	5009 C8	
2023 B8	6001 C1	
2024 B8	6002 C1	
2025 A6	6003 B2	
2026 C7	6004 B2	
2027 A9	6005 C4	
2028 A7	6006 B4	
2032 A5	6007 B4	
2033 B1	6008 B4	
2034 A5	6009 A4	
2035 A3	6010 B4	
3001 B2	6011 B9	
3002 C4	6017 A5	
3003 C4	6018 C7	
3004 A4	6021 B7	
3005 B4	6022 C7	
3006 B4	6023 B7	
3007 B4	6025 C8	
3008 A4	7001 A4	
3009 A4	7002 B4	
3010 C2	7003 C7	

6.3.1 POWER SUPPLY PCB, COPPER TRACK SIDE VIEW



0003 B1	3011 C2	7004 A4
0004 C10	3012 A4	7005 B9
0005 B10	3013 C3	7006 C9
0006 A9	3014 A8	7007 B9
0007 C10	3015 C10	9001 A5
1001 A2	3018 C8	9002 C7
2001 A2	3019 C8	9003 A10
2002 C3	3020 C8	9004 B10
2006 C4	3022 C7	9005 A10
2008 C4	3023 A9	BU-1 A1
2009 A5	3024 B8	SK-4 C1
2010 A4	5025 A9	
2012 B3	5026 C7	
2015 C9	5001 A3	
2017 C9	5002 B5	
2018 C9	5003 A4	
2019 C9	5006 B8	
2020 C10	5007 C8	
2021 B9	5008 A8	
2022 B8	5009 C8	
2023 B8	6001 C1	
2024 B8	6002 C1	
2025 A6	6003 B2	
2026 C7	6004 B2	
2027 A9	6005 C4	
2028 A7	6006 B4	
2032 A5	6007 B4	
2033 B1	6008 B4	
2034 A5	6009 A4	
2035 A3	6010 B4	
3001 B2	6011 B9	
3002 C4	6017 A5	
3003 C4	6018 C7	
3004 A4	6021 B7	
3005 B4	6022 C7	
3006 B4	6023 B7	
3007 B4	6025 C8	
3008 A4	7001 A4	
3009 A4	7002 B4	
3010 C2	7003 C7	

6.3.2 POWER SUPPLY CIRCUIT DIAGRAM

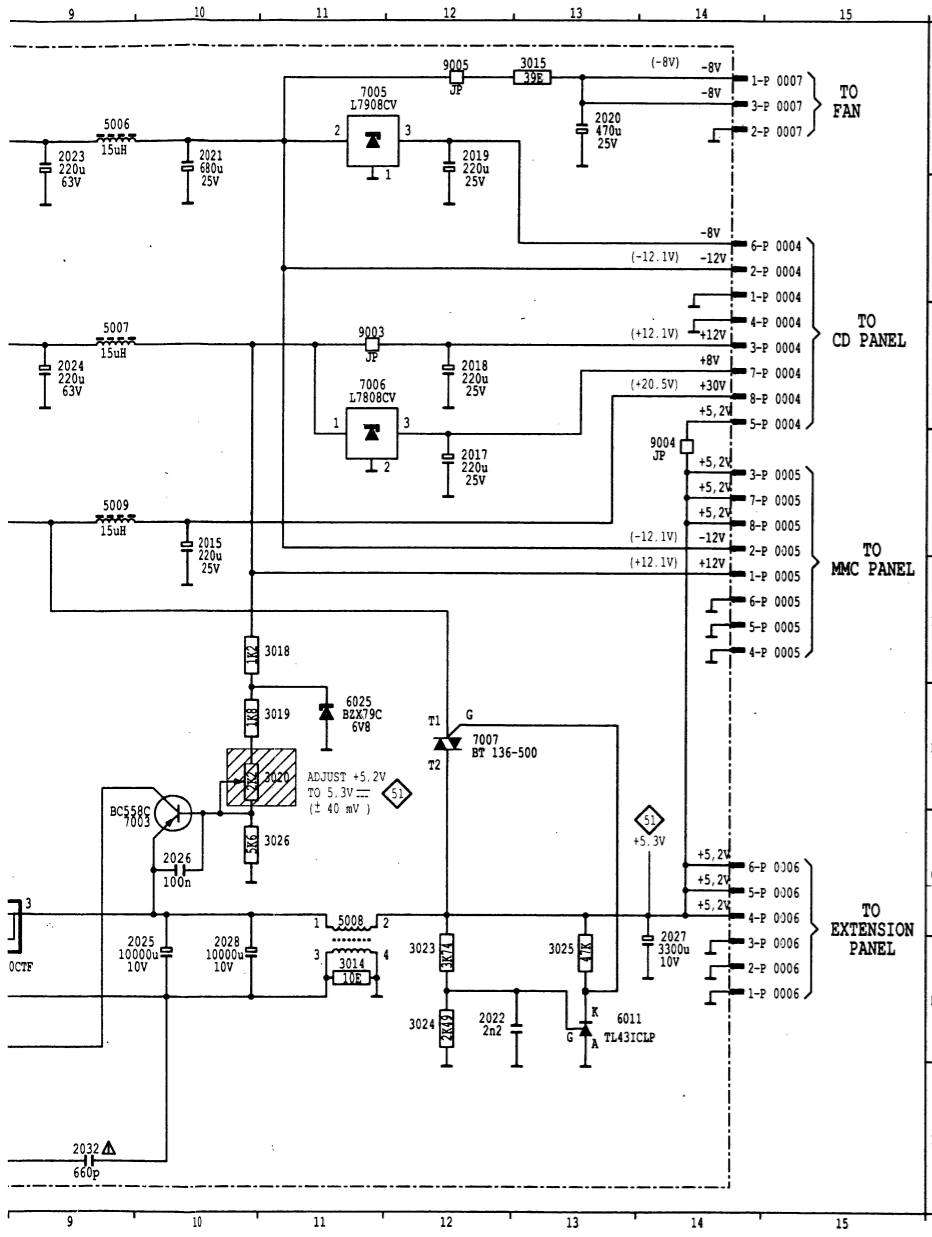


6.3.3 LIST OF ELECTRICAL PARTS POWER SUPPLY

Item	Codenumbr	Description
1001	4822 070 32002	FUSE
2001	5322 121 44271	POLCAP 330NF 250V
2032	4822 126 12056	CER. CAP 470PF 125V
2032	4822 121 70112	CAPACITOR ASSY
3001	4822 116 30069	THERMISTOR
3015	4822 116 21208	VDR
3020	4822 100 10019	TRIM 2K2 OHM LIN
5001	4822 157 63913	CHOKE ASSY CU15D3
5002	4822 146 30956	TRANSFORMER
6001	4822 130 80229	BYD14J
6002	4822 130 80229	BYD14J
6003	4822 130 80229	BYD14J
6004	4822 130 80229	BYD14J
6005	4822 130 31881	BZX79-C3V0
6006	4822 130 34193	BAX14
6007	4822 130 34441	BZX79-C22
6008	4822 130 34193	BAX14
6009	4822 130 80915	BYD74C
6010	4822 130 34193	BAX14
6011	4822 209 81397	TL431CLP
6017	4822 130 10025	CNX82A
6018	4822 130 80915	BYD74C
6021	4822 130 80915	BYD74C
6022	4822 130 80915	BYD74C
6023	4822 130 82553	DIODE PBYR 2540 CTF
6025	4822 130 34278	BZX79-C6V8
7001	4822 130 40959	BC547B
7002	4822 130 62735	BUT12AF
7003	5322 130 60068	BC558C
7004	5322 130 44661	BD227
7005	4822 209 82112	MC7908CT
7006	4822 209 72554	MC7808CT
7007	4822 130 20248	TRIAC BT136-500
A	5322 390 20019	HEATSINK COMPOUND

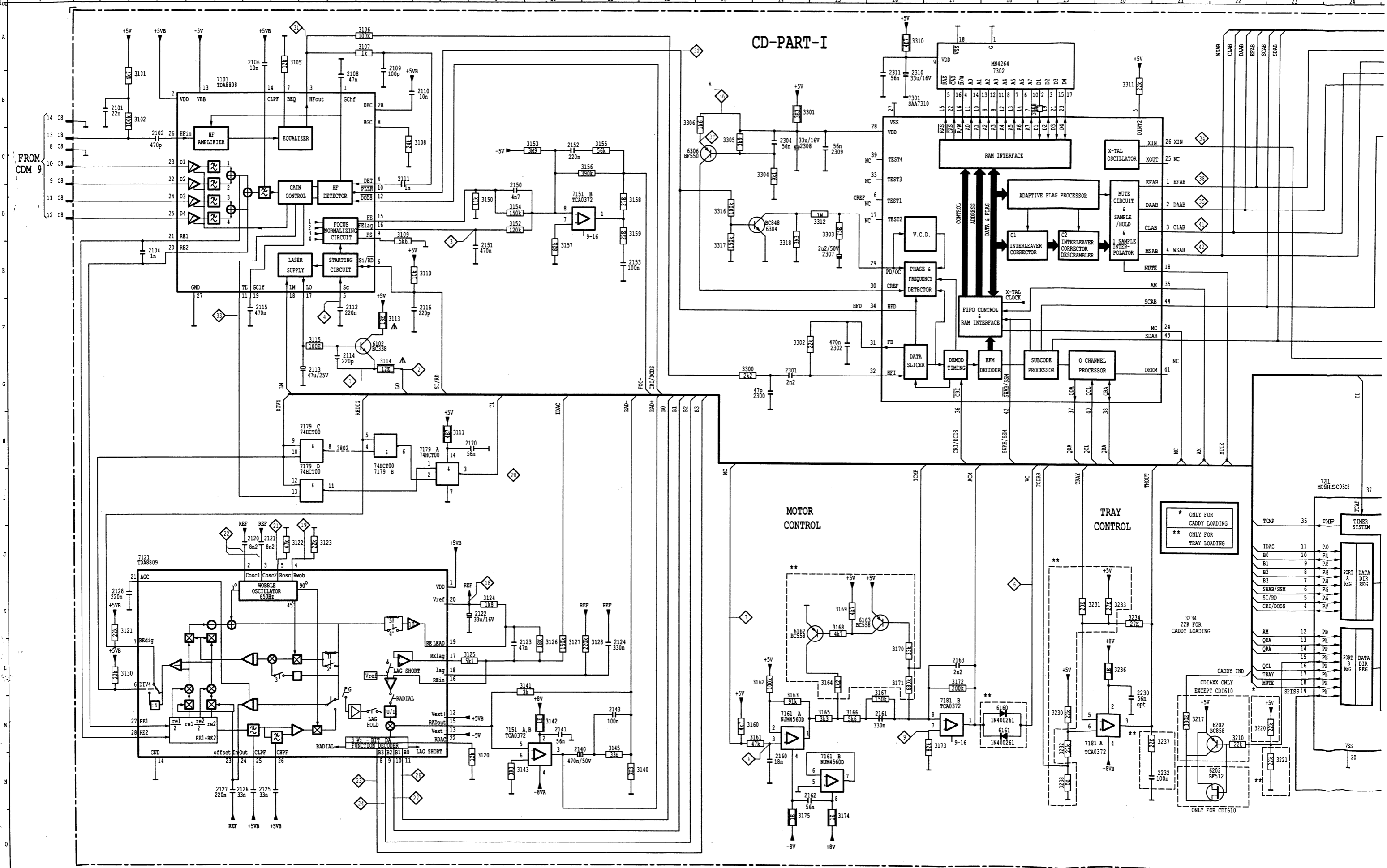
6.3.3 LIST OF ELECTRICAL PARTS POWER SUPPLY

3010	D	6	3015	A13	3023	H12	5003	E	6	6004	C	5	6009	E	7	6021	C	8	7002	D	7	7007	F12
3011	C	6	3018	E11	3024	H12	5006	A	9	6005	D	3	6010	G	6	6022	A	8	7003	G10	9003	C11	
3012	H	5	3019	F11	3025	H13	5007	C	9	6006	F	4	6011	H13	6	6023	C	8	7004	E	6	9004	D14
3013	C	7	3020	F11	3026	G11	5008	G11		6007	F	4	6012	F	8	6025	F11		7005	A11	9005	B12	
3014	H11	3022	H	8	3001	B	3	5009	D	9	6008	H	6	6013	D	8	7001	E	5	7006	C11		

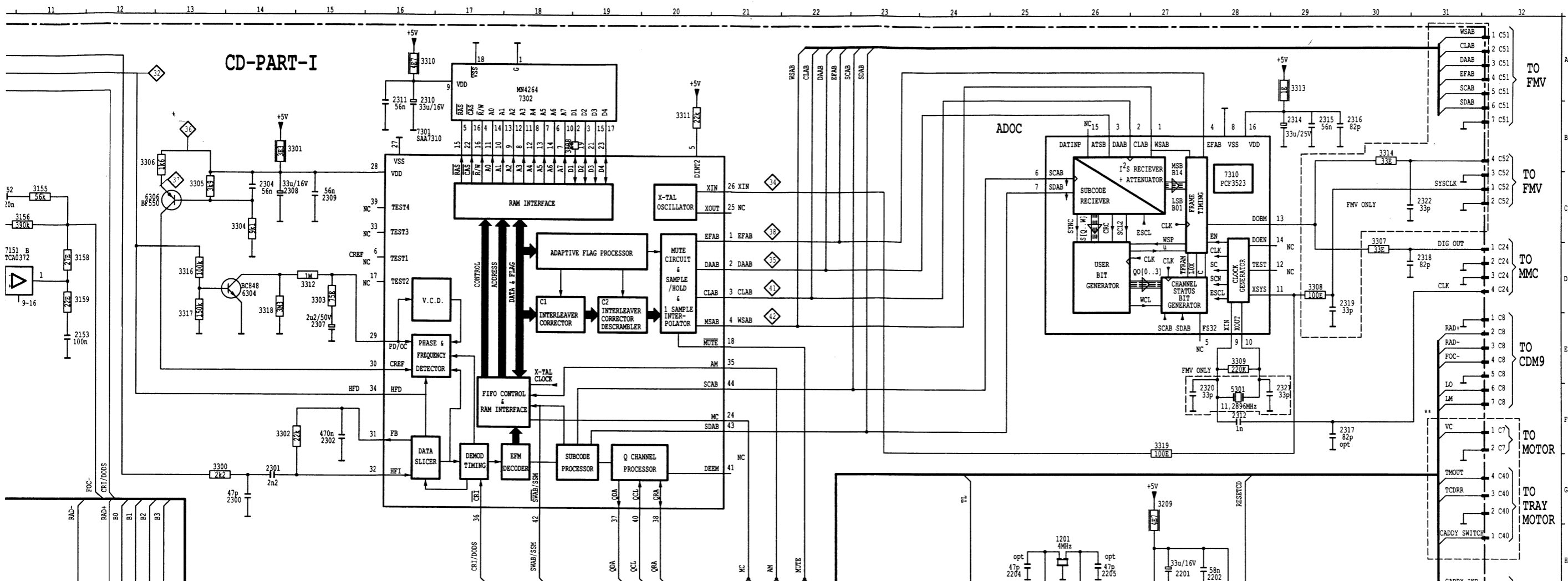


Item	Codenumber	Description
1001	4822 070 32002	FUSE
2001	5322 121 44271	POLCAP 330NF 250V
2032	4822 126 12056	CER. CAP 470PF 125V
2032	4822 121 70112	CAPACITOR ASSY
3001	4822 116 30069	THERMISTOR
3015	4822 116 21208	VDR
3020	4822 100 10019	TRIM.2K2 OHM LIN
5001	4822 157 63913	CHOKE ASSY CU15D3
5002	4822 146 30956	TRANSFORMER
6001	4822 130 80229	BYD14J
6002	4822 130 80229	BYD14J
6003	4822 130 80229	BYD14J
6004	4822 130 80229	BYD14J
6005	4822 130 31881	BZX79-C3V0
6006	4822 130 34193	BAX14
6007	4822 130 34441	BZX79-C22
6008	4822 130 34193	BAX14
6009	4822 130 80915	BYD74C
6010	4822 130 34193	BAX14
6011	4822 209 81397	TL431CLP
6017	4822 130 10025	CNX82A
6018	4822 130 80915	BYD74C
6021	4822 130 80915	BYD74C
6022	4822 130 80915	BYD74C
6023	4822 130 82553	DIODE PBYR 2540 CTF
6025	4822 130 34278	BZX79-C6V8
7001	4822 130 40959	BC547B
7002	4822 130 62735	BUT12AF
7003	5322 130 60068	BC558C
7004	5322 130 44661	BD227
7005	4822 209 82112	MC7908CT
7006	4822 209 72554	MC7808CT
7007	4822 130 20248	TRIAC BT136-500
A	5322 390 20019	HEATSINK COMPOUND

6.4.1 CIRCUIT DIAGRAM CD PART 1

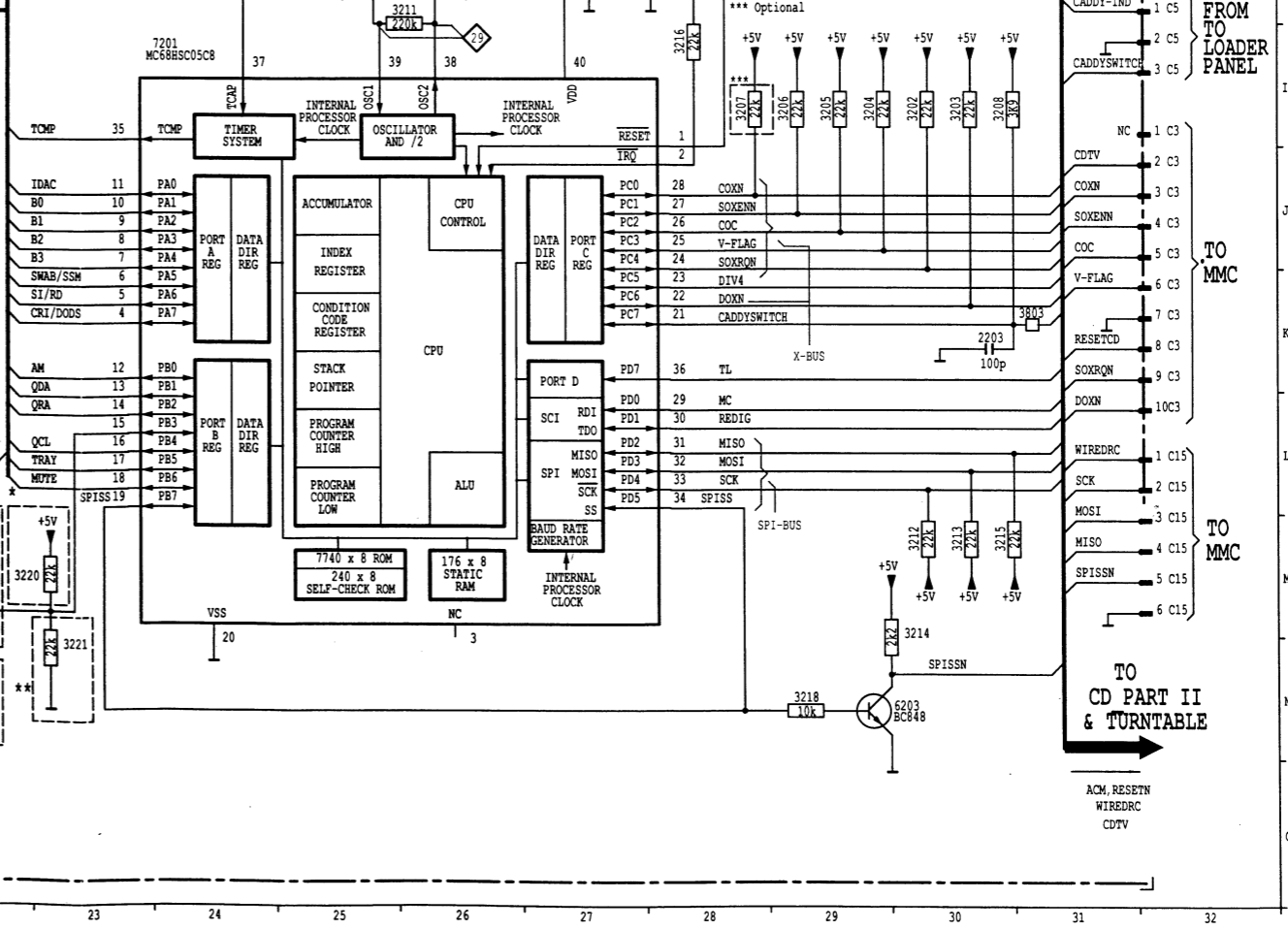
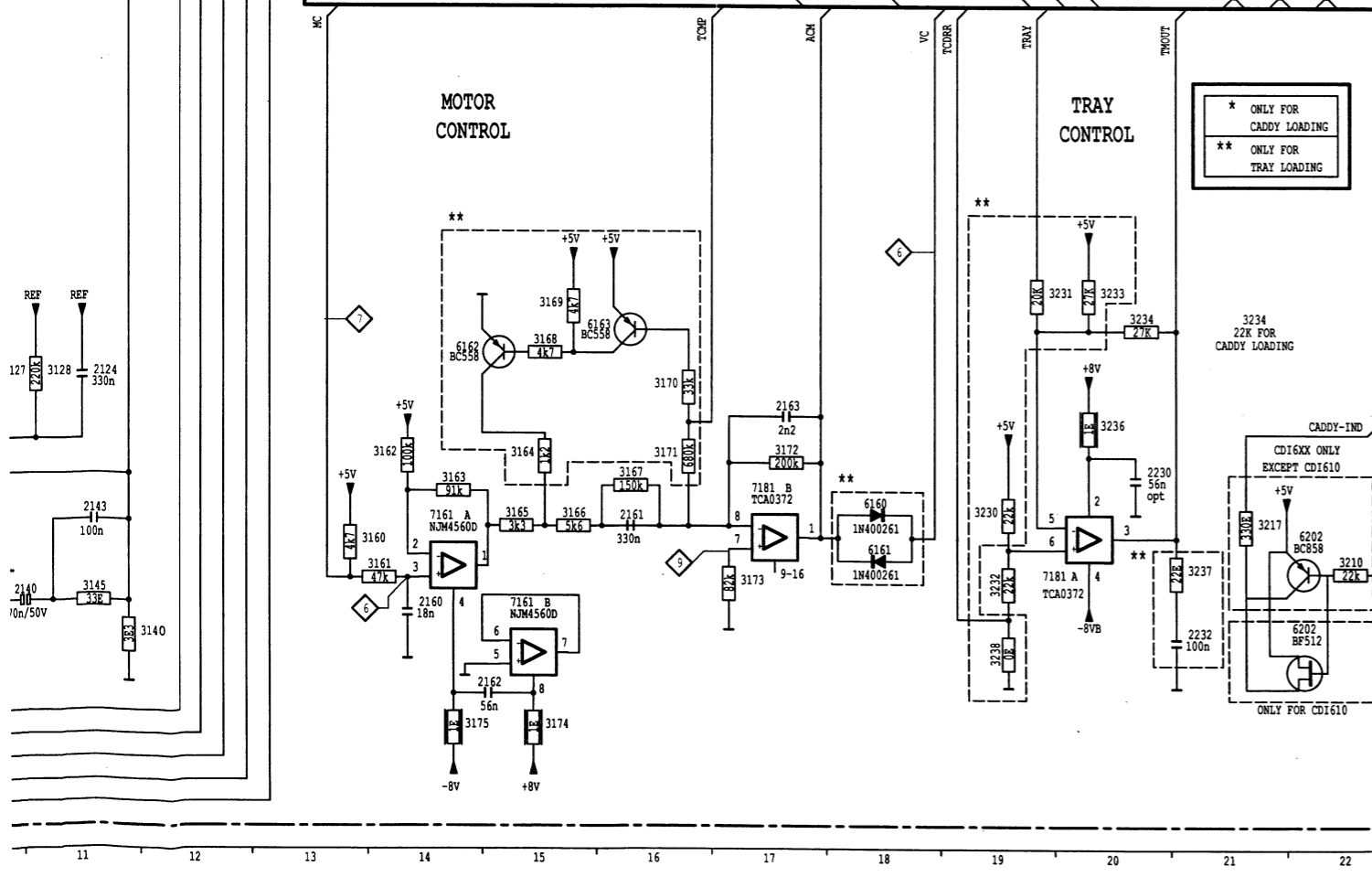


CD-PART-I



MOTOR CONTROL

TRAY CONTROL

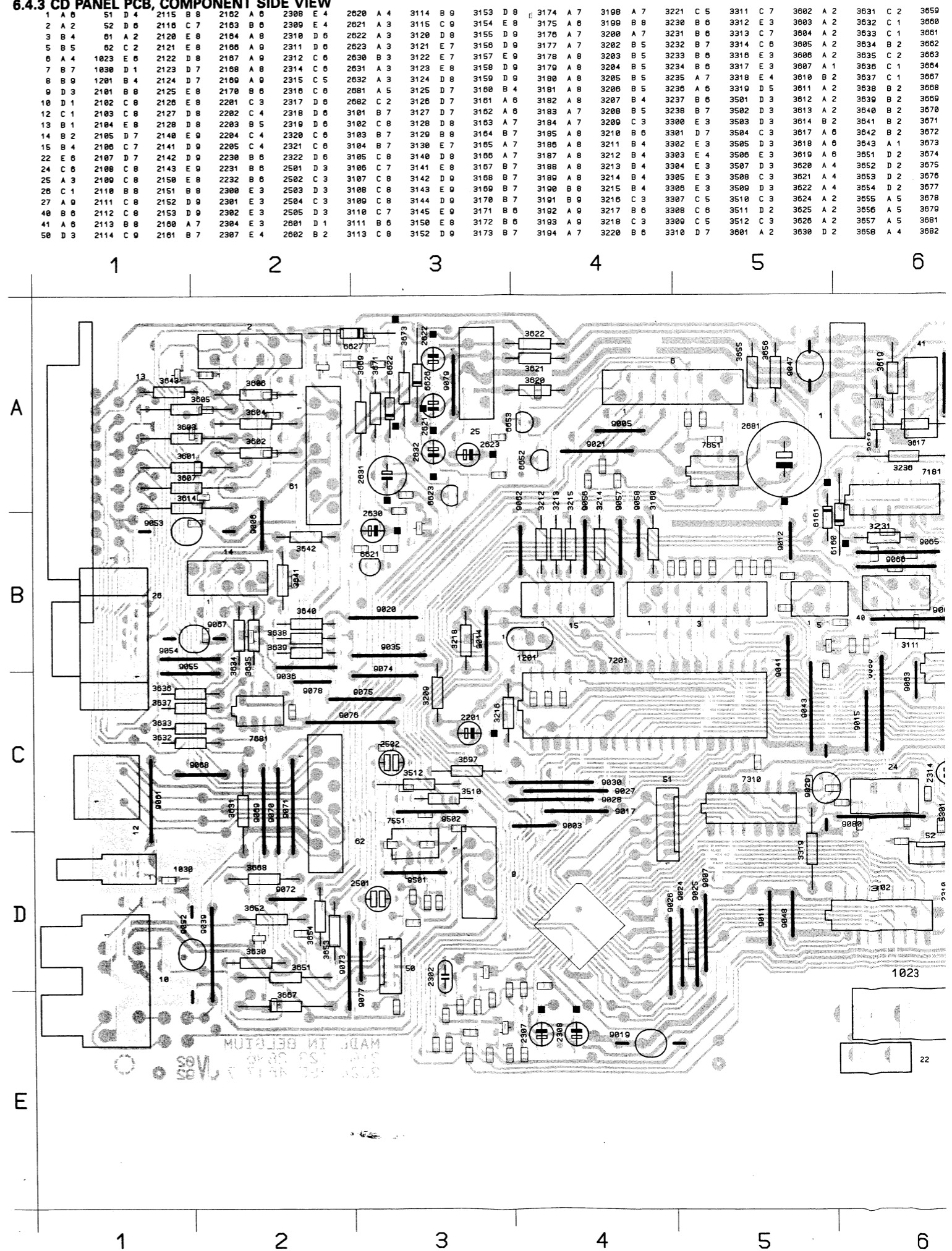


TO FMV
TO FMV
TO MMC
TO CDM9
TO MOTOR
TO TRAY MOTOR
FROM TO LOADER PANEL
TO MMC
TO MMC
TO CD PART II & TURNABLE
ACH, RESETN
WIREDRC
CDTV

6.4.2 LIST OF ELECTRICAL PARTS CD PANEL

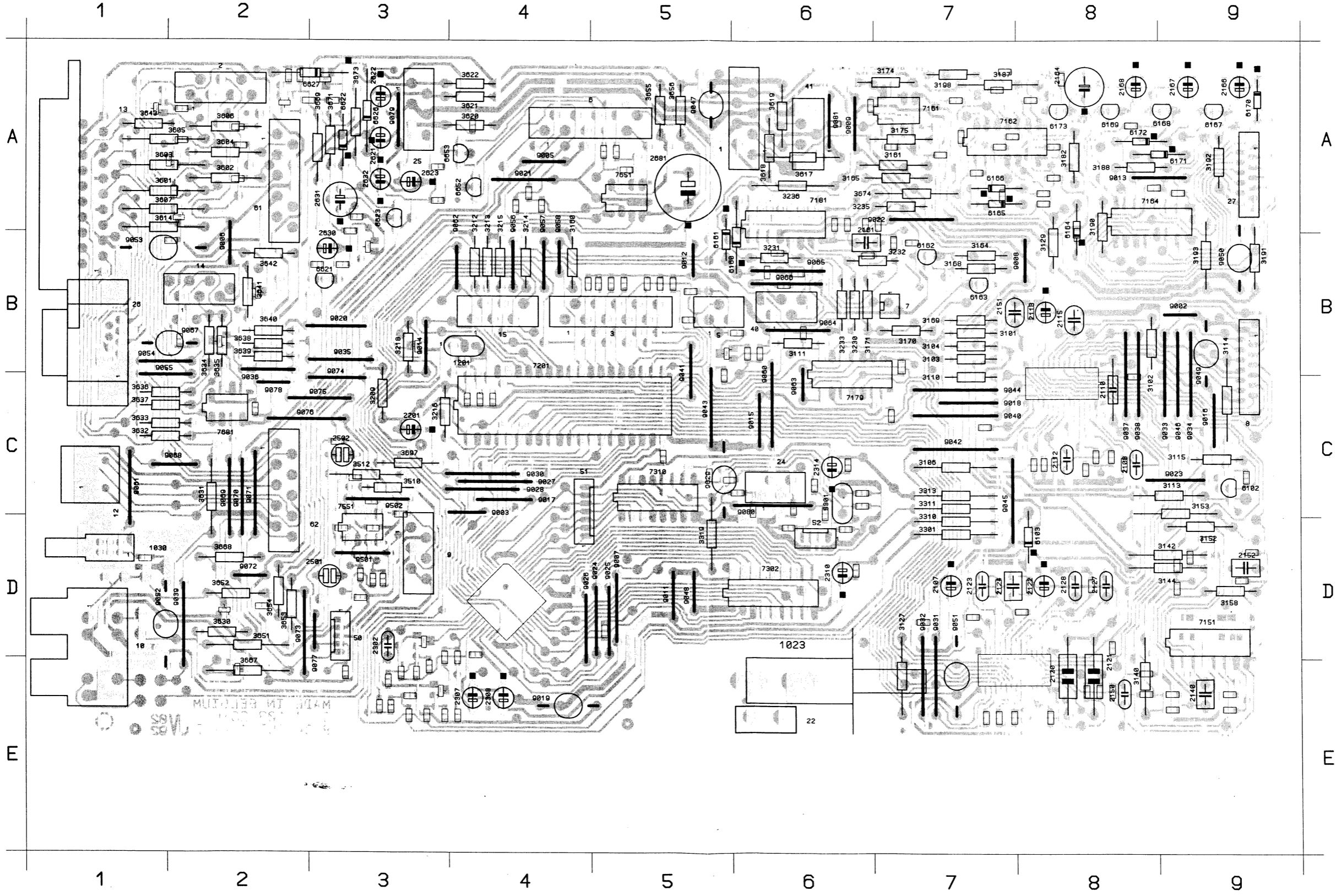
Item	Codenumber	Description
BU-6	4822 267 40857	CS7927-24-401
BU-7	4822 267 20414	CINCH SOCKET 4P
BU-8	4822 267 20414	CINCH SOCKET 4P
BU-9	4822 267 20414	CINCH SOCKET 4P
BU-10	4822 267 20414	CINCH SOCKET 4P
SK-1	4822 276 11309	MAINS-POWER SWITCH
1013	4822 267 60326	SCART CONN. 7087D
1201	4822 242 72527	CRYSTAL 4,000MHZ
3103	4822 052 10478	NFR25 4R7
3111	4822 052 10478	NFR25 4R7
3113	4822 052 10189	NFR25 18R
3114	4822 052 10129	NFR25 12R
3142	4822 052 10108	NFR25 1R0
3144	4822 052 10108	NFR25 1R0
3174	4822 052 10108	NFR25 1R0
3175	4822 052 10108	NFR25 1R0
3187	4822 052 10158	NFR25 1R5
3209	4822 052 10478	NFR25 4R7
3236	4822 052 10108	NFR25 1R0
3235	4822 052 10108	NFR25 1R0
3301	4822 052 10338	NFR25 3R3
3310	4822 052 10478	NFR25 4R7
3313	4822 052 10108	NFR25 1R0
3620	4822 052 10158	NFR25 1R5
3621	4822 052 10228	NFR25 2R2
3622	4822 052 10228	NFR25 2R2
3655	4822 052 10229	NFR25 22R
3656	4822 052 10229	NFR25 22R
3900	4822 052 10339	NFR25 33R PM5
6102	4822 130 44121	BC338
6161	5322 130 30684	1N4002
6162	4822 130 40941	BC558
6163	4822 130 40941	BC558
6203	4822 130 61207	BC848
6304	4822 130 61207	BC848
6306	4822 130 42131	BF550
6607	4822 130 61207	BC848
6608	4822 130 61207	BC848
6609	4822 130 61207	BC848
6620	4822 130 61207	BC848
6621	4822 130 40941	BC558
6622	5322 130 30684	1N4002
6623	4822 130 40941	BC558
6624	5322 130 41982	BC848B
6625	5322 130 41982	BC848B
6626	4822 130 30621	1N4148
6627	4822 130 30621	1N4148
6640	5322 130 41983	BC858B
6641	5322 130 41982	SMTRANS BC848B
6652	4822 130 40958	BC338-25
6653	4822 130 40958	BC338-25
6654	4822 130 42675	BC818
6655	4822 130 42675	BC818
7101	4822 209 73234	TDA8808T/C3
7121	4822 209 73235	TDA8809T/C2
7151	4822 209 72587	TCA0372DP2
7161	4822 209 83274	NJM4560D
7179	5322 209 11105	PC74HCT00P
7181	4822 209 72587	TCA0372DP2
7201	4822 209 30995	MC68HC05C8/SERVO PROC/2.1
7202	4822 209 70422	MN4264-15
7301	4822 209 61759	SAA7310GP/H5
7302	4822 209 70422	MN4264-15
7310	4822 209 62588	PCF3523P
7551	5322 209 86234	NE5532N
7651	4822 209 82362	NJM4556D
7681	4822 209 83163	LM833N

6.4.3 CD PANEL PCB, COMPONENT SIDE VIEW



6.4.3 CD PANEL PCB, COMPONENT SIDE VIEW

1	A 6	51	D 4	2115	B 8	2102	A 6	2308	E 4	2020	A 4	3114	B 9	3153	D 8	3174	A 7	3198	A 7	3221	C 5	3311	C 7	3602	A 2	3631	C 2	3650	A 5	3690	B 3	6172	A 8	6654	D 2	9007	D 5	9029	D 5	9050	B 9	9072	D 2
2	A 2	52	D 6	2116	C 7	2103	B 6	2309	E 4	2021	A 3	3115	C 9	3154	E 8	3175	A 6	3199	B 8	3230	B 6	3312	E 3	3603	A 2	3632	C 1	3660	A 4	3697	C 3	6173	A 8	6655	E 2	9008	B 8	9030	C 3	9051	E 7	9073	E 2
3	B 4	61	A 2	2120	E 8	2104	A 8	2310	D 6	2022	A 3	3120	D 8	3155	D 9	3176	A 7	3200	A 7	3231	B 6	3313	C 7	3604	A 2	3633	C 1	3661	A 5	3698	C 7	6202	B 5	7101	C 8	9009	A 6	9031	D 7	9052	D 2	9074	C 3
5	B 5	62	C 2	2121	E 8	2106	A 9	2311	D 6	2023	A 3	3121	E 7	3156	D 9	3177	A 7	3202	B 5	3232	B 7	3314	C 6	3605	A 2	3634	B 2	3662	A 4	3693	B 5	6203	B 3	7121	E 8	9011	D 5	9032	D 7	9053	B 2	9075	C 2
6	A 4	1023	E 6	2122	D 8	2107	A 9	2312	C 6	2030	B 3	3122	E 7	3157	E 9	3178	A 8	3203	B 5	3233	B 6	3315	E 3	3606	A 2	3635	C 2	3663	A 3	3696	A 8	6304	E 3	7151	E 9	9012	B 5	9033	B 9	9054	B 1	9076	C 2
7	B 7	1030	D 1	2123	D 7	2108	A 8	2314	C 6	2031	A 3	3123	E 8	3158	D 9	3179	A 8	3204	B 5	3234	B 6	3317	E 3	3607	A 1	3636	C 1	3664	A 3	3698	D 5	6308	D 3	7161	A 7	9013	A 8	9034	B 9	9055	C 1	9077	D 3
8	B 9	1201	B 4	2124	D 7	2109	A 9	2315	C 5	2032	A 3	3124	D 8	3159	D 9	3180	A 8	3205	A 7	3235	A 7	3318	E 4	3608	B 2	3637	C 1	3667	E 2	5301	D 8	6607	A 2	7162	A 7	9014	B 3	9035	B 3	9056	B 4	9078	C 2
9	D 3	2101	B 8	2125	E 8	2170	B 6	2316	C 6	2091	A 5	3125	D 7	3160	B 4	3181	A 8	3206	B 5	3236	A 6	3319	D 5	3611	A 2	3638	B 2	3668	D 2	6102	C 9	6608	A 2	7104	B 8	9015	C 6	9036	C 2	9057	B 4	9079	A 3
10	D 1	2102	C 8	2126	E 8	2201	C 3	2317	D 6	2092	C 2	3126	D 7	3161	A 6	3182	A 8	3207	B 4	3237	B 6	3301	D 3	3612	A 2	3639	B 2	3669	A 3	6103	D 8	6609	A 1	7179	C 6	9016	C 9	9037	B 8	9058	B 4	9080	C 6
12	C 1	2103	C 8	2127	D 8	2202	C 4	2318	D 6	3101	B 7	3127	D 7	3162	A 6	3183	A 7	3208	B 5	3238	B 7	3302	D 3	3613	A 2	3640	B 2	3670	B 3	6104	A 6	6620	B 3	7181	B 6	9017	C 4	9038	B 8	9059	B 6	9081	A 6
13	B 1	2104	E 8	2128	D 8	2203	B 5	2319	D 6	3102	C 8	3128	D 8	3163	A 7	3184	A 7	3209	C 3	3300	E 3	3503	D 3	3614	B 2	3641	B 2	3671	A 3	6101	B 5	6621	B 3	7201	C 4	9018	C 7	9039	D 2	9061	C 1	9501	D 3
14	B 2	2105	D 7	2140	E 9	2204	C 4	2320	C 6	3103	B 7	3129	B 8	3164	B 7	3185	A 8	3210	B 6	3301	D 7	3504	C 3	3615	A 6	3642	B 2	3672	B 3	6102	B 7	6622	A 3	7301	D 4	9019	E 5	9040	C 7	9062	B 4	9502	C 3
15	A 4	2106	C 7	2141	D 9	2205	C 4	2321	C 6	3104	A 7	3130	E 7	3165	A 7	3186	A 8	3211	B 4	3302	E 3	3505	D 3	3616	A 6	3643	A 1	3673	A 3	6103	B 7	6623	A 3	7302	D 6	9020	B 3	9041	C 5	9063	C 6		
22	E 6	2107	D 7	2142	D 9	2230	B 6	2322	D 6	3105	C 8	3140	D 8	3166	A 7	3187	A 8	3212	B 4	3303	E 4	3506	F 3	3617	A 6	3644	D 2	3674	A 7	6104	A 8	6624	A 3	7310	D 5	9021	A 4	9042	C 7	9064	B 6		
24	C 6	2108	C 8	2143	E 9	2231	B 6	2501	D 3	3106	C 7	3141	E 8	3167	B 7	3188	A 8	3213	B 4	3304	E 3	3507	D 3	3618	A 6	3645	A 1	3675	A 3	6105	A 7	6625	A 2	7551	D 3	9022	A 7	9043	C 5	9065	B 6		
25	A 3	2150	C 8	2150	E 8	2232	B 6	2502	C 3	3107	C 8	3142	D 9	3168	B 7	3189	A 8	3214	B 4	3305	E 3	3508	C 3	3619	A 6	3646	D 2	3676	A 3	6106	A 8	6626	A 3	7651	A 5	9023	C 8	9044	C 7	9066	B 6		
26	C 1	2110	B 8	2151	B 8	2300	E 3	2503	D 3	3108	C 8	3143	C 9	3169	B 7	3190	B 8	3215	B 4	3306	E 3	3509	D 3	3620	A 4	3652	D 2	3675	A 3	6105	A 7	6625	A 2	7551	D 3	9024	A 7	9045	C 7	9067	B 1		
27	A 9	2111	C 8	2152	D 9	2301	E 3	2504	C 3	3109	C 8	3144	D 9	3170	B 7	3191	B 9	3216	C 3	3307	C 5	3510	C 3	3622	A 4	3654	D 2	3677	A 2	6107	A 9	6627	A 2	7681	C 2	9024	D 5	9045	C 7	9067	B 1		
40	B 6	2112	C 8	2153	D 9	2302	E 3	2505	D 3	3110	C 7	3145	E 9	3171	B 6	3192	A 9	3217	B 6	3308	C 6	3511	D 2	3623	A 2	3655	A 5	3678	A 2	6108	A 8	6628	B 9	9025	E 5	9046	B 9	9068	C 1				
41	A 6	2113	B 8	2154	A 7	2304	E 3	2506	D 3	3111	C 7	3145	E 9	3171	B 6	3192	A 9	3217	B 6	3308	C 6	3511	D 2	3623	A 2	3655	A 5	3678	A 2	6108	A 8	6641	B 2	9003	D 4	9026	D 4	9047	A 5	9069	D 2		
50	D 3	2114	C 9	2151	B 7	2307	E 4	2602	B 2	3113	C 8	3152	D 9	3173	B 7	3194	A 7	3220	B 6	3310	D 7	3512	C 3	3624	A 2	3657	A 5	3679	A 1	6170	A 9	6652	A 4	9005	A 4	9027	C 4	9048	D 5	9070	D 2		
				2151	B 7	2307	E 4	2602	B 2	3113	C 8	3152	D 9	3173	B 7	3194	A 7	3220	B 6	3310	D 7	3512	C 3	3624	A 2	3657	A 5	3679	A 1	6170	A 9	6653	A 4	9006	A 2	9028	C 3	9049	B 9	9071	D 2		

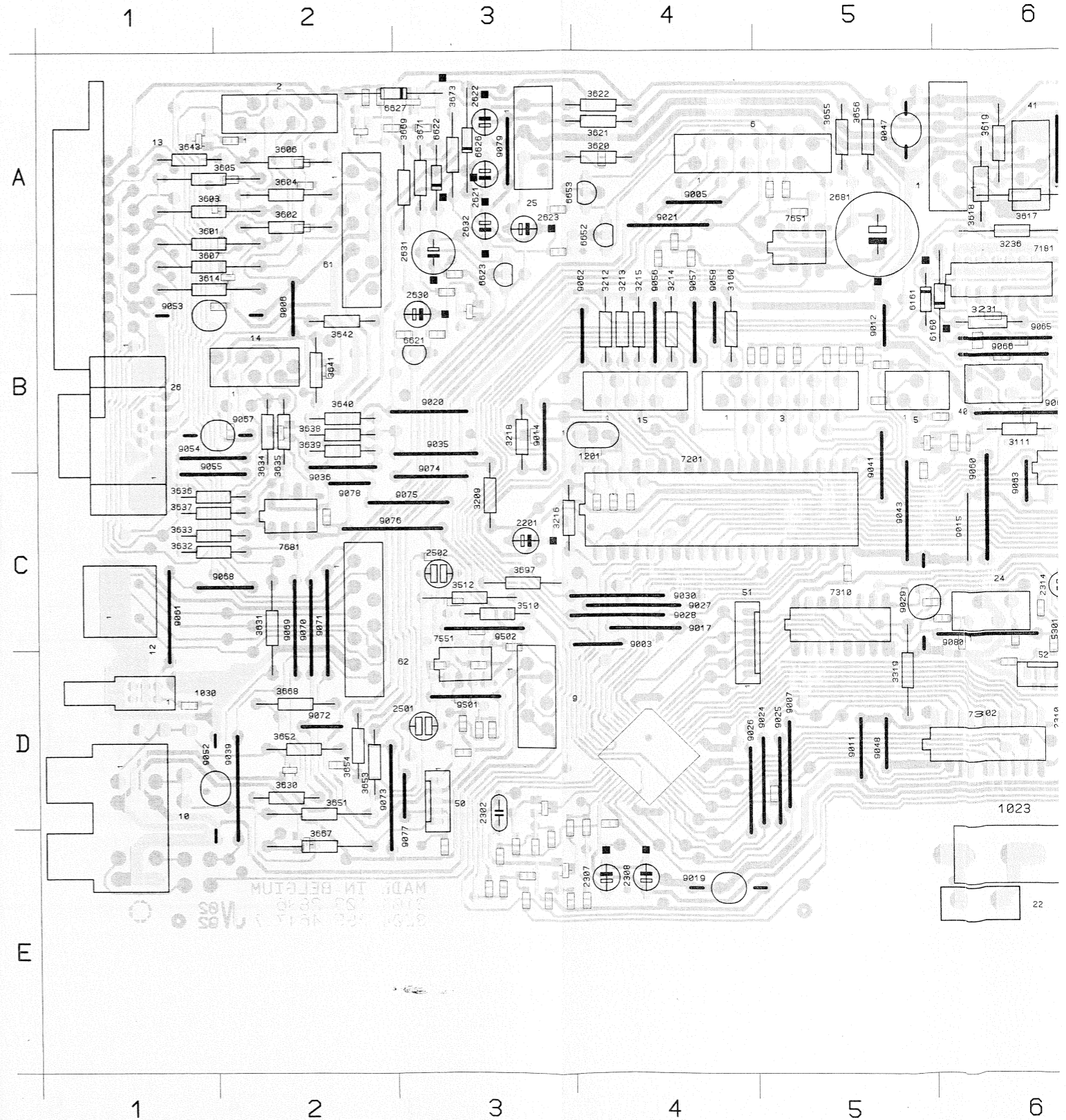


6.4.2 LIST OF ELECTRICAL PARTS CD PANEL

Item	Codenumber	Description
BU-6	4822 267 40857	CS7927-24-401
BU-7	4822 267 20414	CINCH SOCKET 4P
BU-8	4822 267 20414	CINCH SOCKET 4P
BU-9	4822 267 20414	CINCH SOCKET 4P
BU-10	4822 267 20414	CINCH SOCKET 4P
SK-1	4822 276 11309	MAINS-POWER SWITCH
1013	4822 267 60326	SCART CONN. 7087D
1201	4822 242 72527	CRYSTAL 4,000MHZ
3103	4822 052 10478	NFR25 4R7
3111	4822 052 10478	NFR25 4R7
3113	4822 052 10189	NFR25 18R
3114	4822 052 10129	NFR25 12R
3142	4822 052 10108	NFR25 1R0
3144	4822 052 10108	NFR25 1R0
3174	4822 052 10108	NFR25 1R0
3175	4822 052 10108	NFR25 1R0
3187	4822 052 10158	NFR25 1R5
3209	4822 052 10478	NFR25 4R7
3236	4822 052 10108	NFR25 1R0
3235	4822 052 10108	NFR25 1R0
3301	4822 052 10338	NFR25 3R3
3310	4822 052 10478	NFR25 4R7
3313	4822 052 10108	NFR25 1R0
3620	4822 052 10158	NFR25 1R5
3621	4822 052 10228	NFR25 2R2
3622	4822 052 10228	NFR25 2R2
3655	4822 052 10229	NFR25 22R
3656	4822 052 10229	NFR25 22R
3900	4822 052 10339	NFR25 33R PM5
6102	4822 130 44121	BC338
6161	5322 130 30684	1N4002
6162	4822 130 40941	BC558
6163	4822 130 40941	BC558
6203	4822 130 61207	BC848
6304	4822 130 61207	BC848
6306	4822 130 42131	BF550
6607	4822 130 61207	BC848
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6621	4822 130 40941	BC558
6622	5322 130 30684	1N4002
6623	4822 130 40941	BC558
6624	5322 130 41982	BC848B
6625	5322 130 41982	BC848B
6626	4822 130 30621	1N4148
6627	4822 130 30621	1N4148
6640	5322 130 41983	BC858B
6641	5322 130 41982	SMTRANS BC848B
6652	4822 130 40958	BC338-25
6653	4822 130 40958	BC338-25
6654	4822 130 42675	BC818
6655	4822 130 42675	BC818
7101	4822 209 73234	TDA8808T/C3
7121	4822 209 73235	TDA8809T/C2
7151	4822 209 72587	TCA0372DP2
7161	4822 209 83274	NJM4560D
7179	5322 209 11105	PC74HCT00P
7181	4822 209 72587	TCA0372DP2
7201	4822 209 30995	MC68HC05C8/SERVO PROC/2.1
7202	4822 209 70422	MN4264-15
7301	4822 209 61759	SAA7310GP/H5
7302	4822 209 70422	MN4264-15
7310	4822 209 62588	PCF3523P
7551	5322 209 86234	NE5532N
7651	4822 209 82362	NJM4556D
7681	4822 209 83163	LM833N

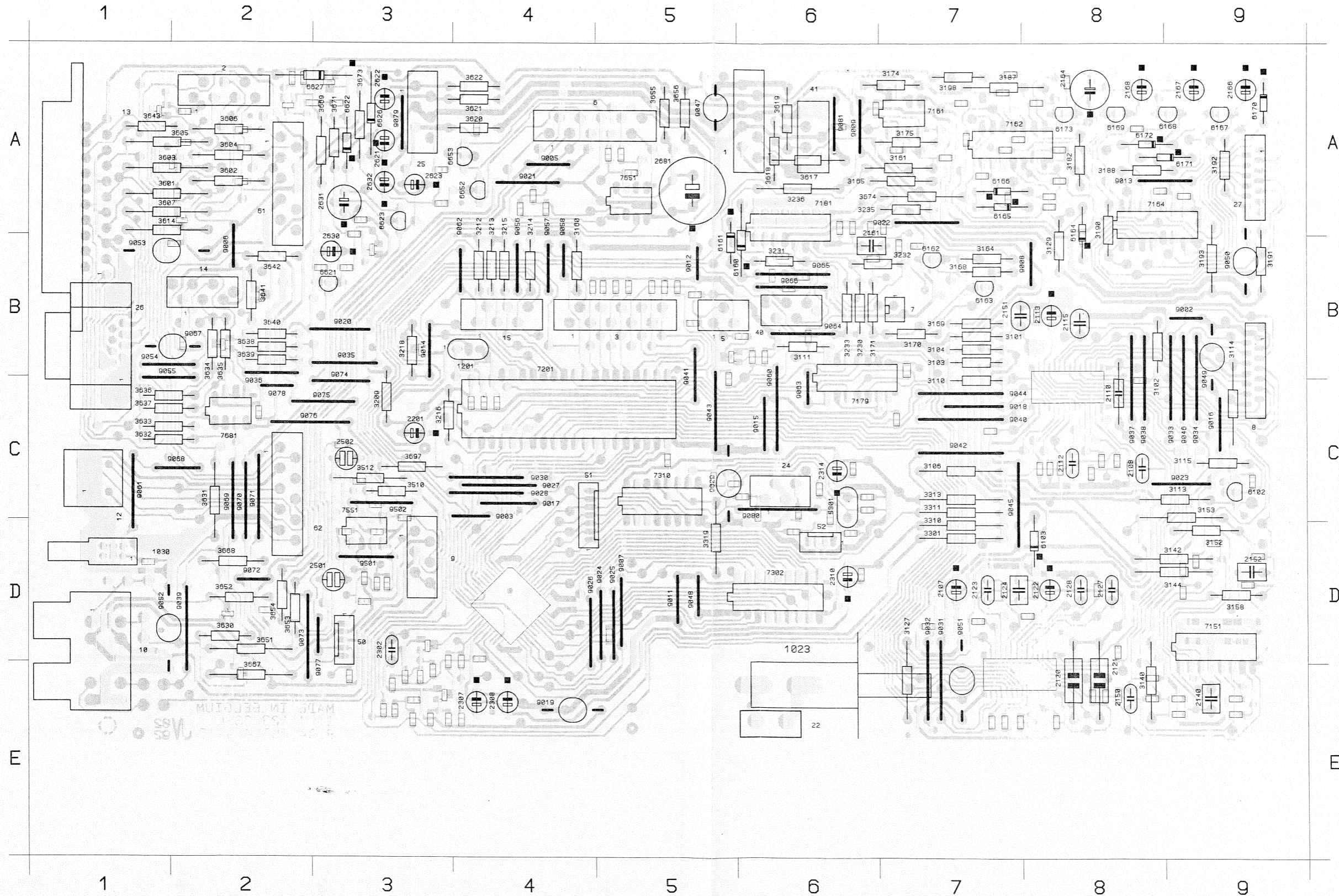
6.4.3 CD PANEL PCB, COMPONENT SIDE VIEW

1	A 6	51	D 4	2115	B 8	2152	A 8	2308	E 4	2620	A 4	3114	B 9	3153	D 8	3174	A 7	3198	A 7	3221	C 5	3311	C 7	3682	A 2	3631	C 2	3650
2	A 2	52	D 6	2116	C 7	2163	B 6	2309	E 4	2621	A 3	3115	C 9	3154	E 8	3175	A 6	3199	B 8	3230	B 6	3312	E 3	3683	A 2	3632	C 1	3650
3	B 4	61	A 2	2120	E 8	2164	A 8	2310	D 5	2622	A 3	3120	D 8	3155	D 9	3176	A 7	3202	A 7	3231	B 6	3313	C 7	3684	A 2	3633	C 1	3651
5	B 5	62	C 2	2121	E 8	2166	A 9	2311	D 6	2623	A 3	3121	E 7	3156	D 9	3177	A 7	3202	B 5	3232	B 7	3314	C 6	3685	A 2	3634	B 2	3652
6	A 4	1023	E 6	2122	D 8	2167	A 9	2312	C 6	2630	B 3	3122	E 7	3157	E 9	3178	A 8	3203	B 5	3233	B 6	3316	E 9	3686	A 2	3635	C 2	3653
7	B 7	1030	D 1	2123	D 7	2168	A 8	2314	C 6	2631	A 3	3123	E 8	3158	D 9	3179	A 8	3204	B 5	3234	B 6	3317	E 9	3687	A 1	3636	C 1	3654
8	B 9	1201	B 4	2124	D 7	2169	A 9	2315	C 5	2632	A 3	3124	D 8	3159	D 9	3180	A 8	3205	B 5	3235	A 7	3318	E 9	3688	A 2	3637	C 1	3657
9	D 3	2101	B 8	2125	E 8	2170	B 6	2316	C 6	2681	A 5	3125	D 7	3160	B 4	3181	A 8	3206	B 5	3236	A 6	3319	E 9	3689	A 1	3638	B 2	3658
10	D 1	2102	C 8	2126	E 8	2201	C 3	2317	D 6	2682	C 2	3126	D 7	3161	A 6	3182	A 8	3207	B 4	3237	B 6	3501	D 3	3690	A 2	3639	B 2	3659
12	C 1	2103	C 8	2127	D 8	2202	C 4	2318	D 6	3101	B 7	3127	D 7	3162	A 6	3183	A 7	3208	B 5	3238	B 7	3502	D 3	3691	A 2	3640	B 2	3670
13	B 1	2104	E 8	2128	D 8	2203	B 5	2319	D 6	3102	C 8	3128	D 8	3163	A 7	3184	A 7	3209	C 3	3300	E 3	3503	D 3	3692	C 3	3641	B 2	3671
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50	D 3	2114	C 9	2161	B 7	2307	E 4	2602	B 2	3113	C 8	3152	D 9	3173	B 7	3194	A 7	3220	B 6	3310	D 7	3601	A 2	3630	D 2	3650	A 4	3682



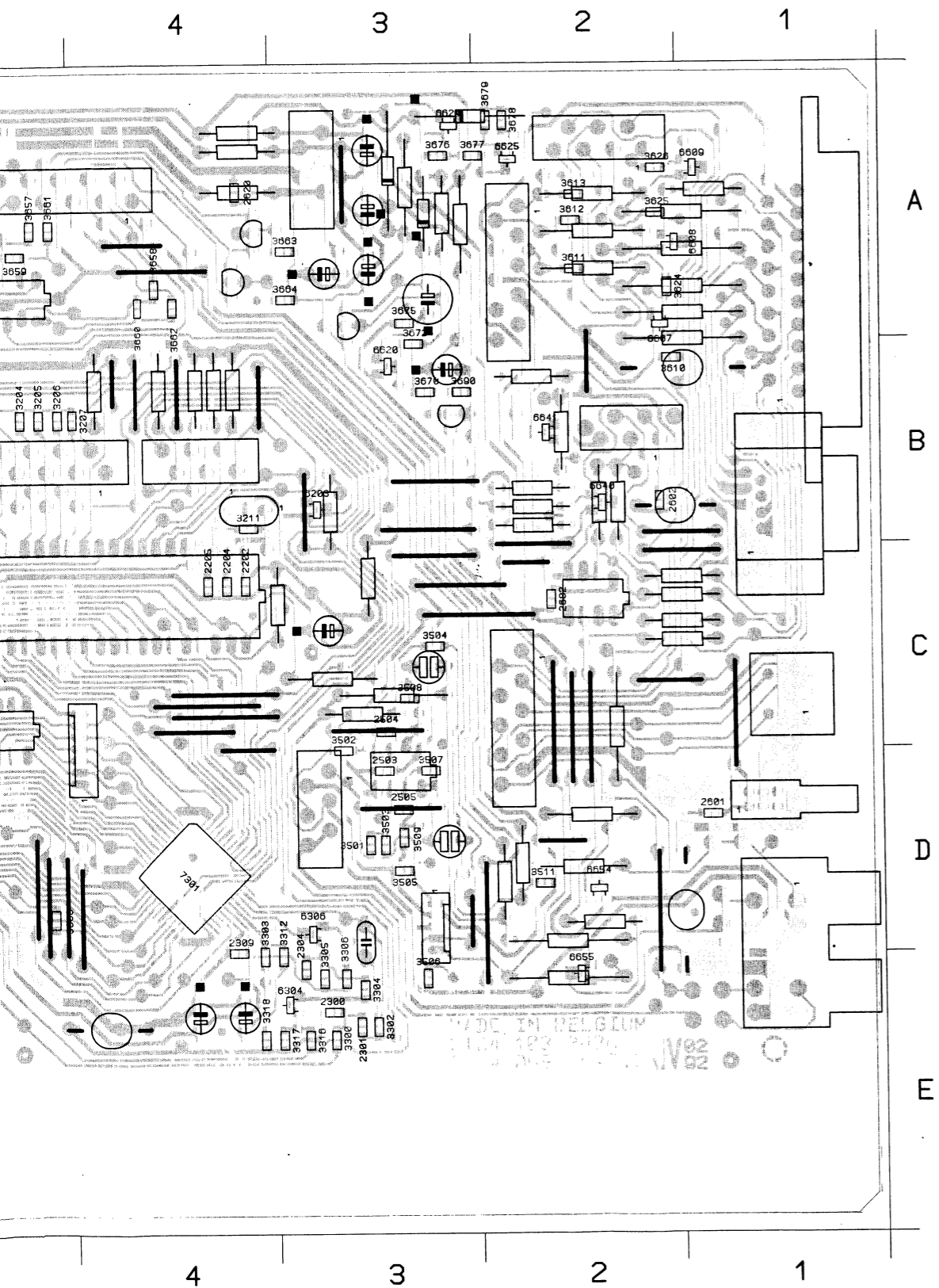
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22	E 6	2107	D 7	2142	D 9	2230	B 6	2322	D 6	3105	C 8	3140	D 8	3166	A 7	3187	A 8	3212	B 4	3303	E 3	3506	E 3	3617	A 6	3644	D 2	3674	A 7	6164	A 8	6624	A 3	7310	D 5	9021	A 4	9042	C 7	9064	B 6		
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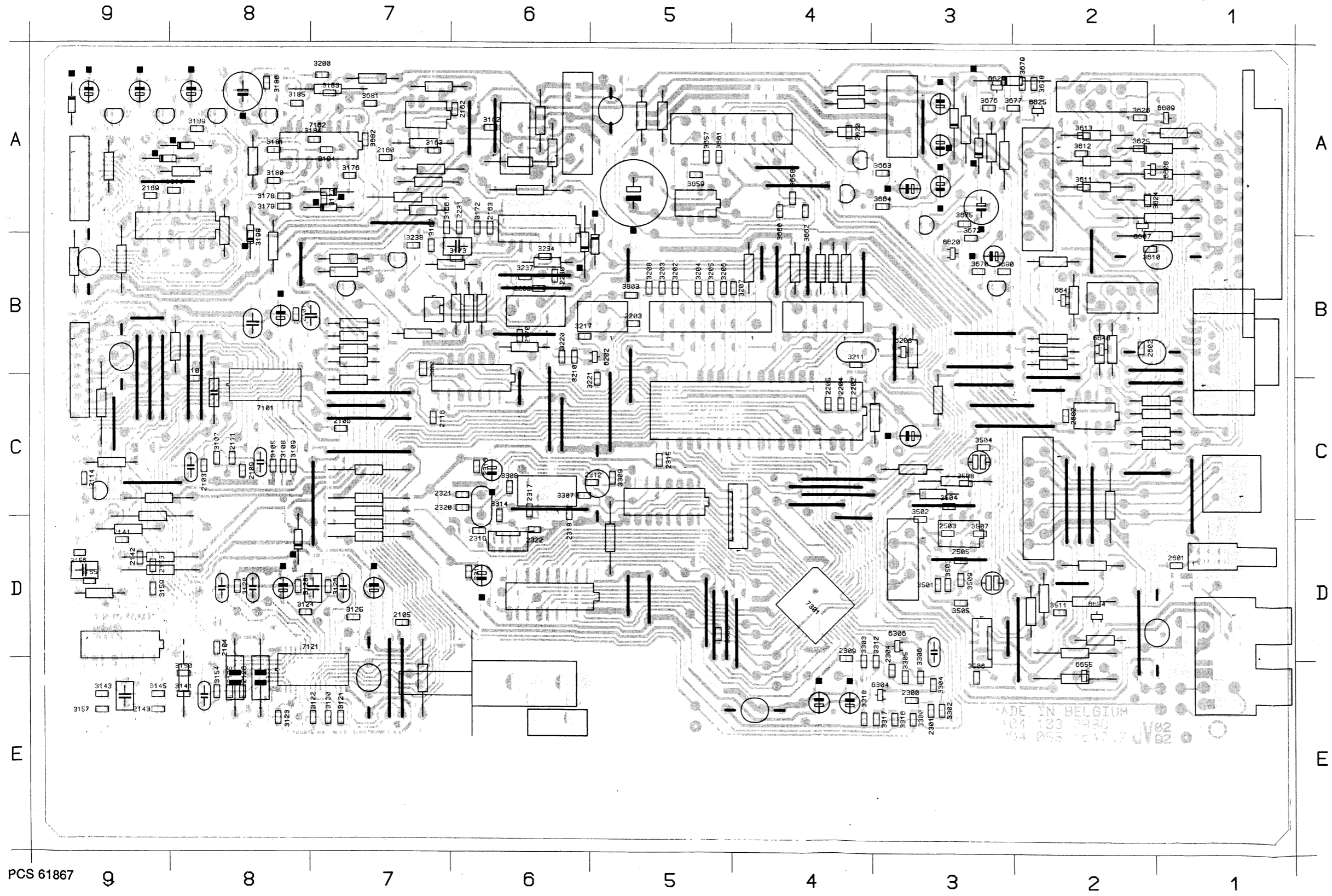
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Item	Codenummer	Description
BU-6	4822 267 40857	CS7927-24-401
BU-7	4822 267 20414	CINCH SOCKET 4P
BU-8	4822 267 20414	CINCH SOCKET 4P
BU-9	4822 267 20414	CINCH SOCKET 4P
BU-10	4822 267 20414	CINCH SOCKET 4P
SK-1	4822 276 11309	MAINS-POWER SWITCH
1013	4822 267 60326	SCART CONN. 7087D
1201	4822 242 72527	CRYSTAL 4,000MHZ
3103	4822 052 10478	NFR25 4R7
3111	4822 052 10478	NFR25 4R7
3113	4822 052 10189	NFR25 18R
3114	4822 052 10129	NFR25 12R
3142	4822 052 10108	NFR25 1R0
3144	4822 052 10108	NFR25 1R0
3174	4822 052 10108	NFR25 1R0
3175	4822 052 10108	NFR25 1R0
3187	4822 052 10158	NFR25 1R5
3209	4822 052 10478	NFR25 4R7
3236	4822 052 10108	NFR25 1R0
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3301	4822 052 10338	NFR25 3R3
3310	4822 052 10478	NFR25 4R7
3313	4822 052 10108	NFR25 1R0
3620	4822 052 10158	NFR25 1R5
3621	4822 052 10228	NFR25 2R2
3622	4822 052 10228	NFR25 2R2
3655	4822 052 10229	NFR25 22R
3656	4822 052 10229	NFR25 22R
3900	4822 052 10339	NFR25 33R PM5
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6161	5322 130 30684	1N4002
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6655	4822 130 42675	BC818
7101	4822 209 73234	TDA8808T/C3
7121	4822 209 73235	TDA8809T/C2
7151	4822 209 72587	TCA0372DP2
7161	4822 209 83274	NJM4560D
7179	5322 209 11105	PC74HCT00P
7181	4822 209 72587	TCA0372DP2
7201	4822 209 30995	MC68HC05C8/SERVO PROC/2.1
7202	4822 209 70422	MN4264-15
7301	4822 209 61759	SAA7310GP/H5
7302	4822 209 70422	MN4264-15
7310	4822 209 62588	PCF3523P
7551	5322 209 86234	NE5532N
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6.4.3 CD PANEL PCB, COPPER TRACK/SMD SIDE VIEW

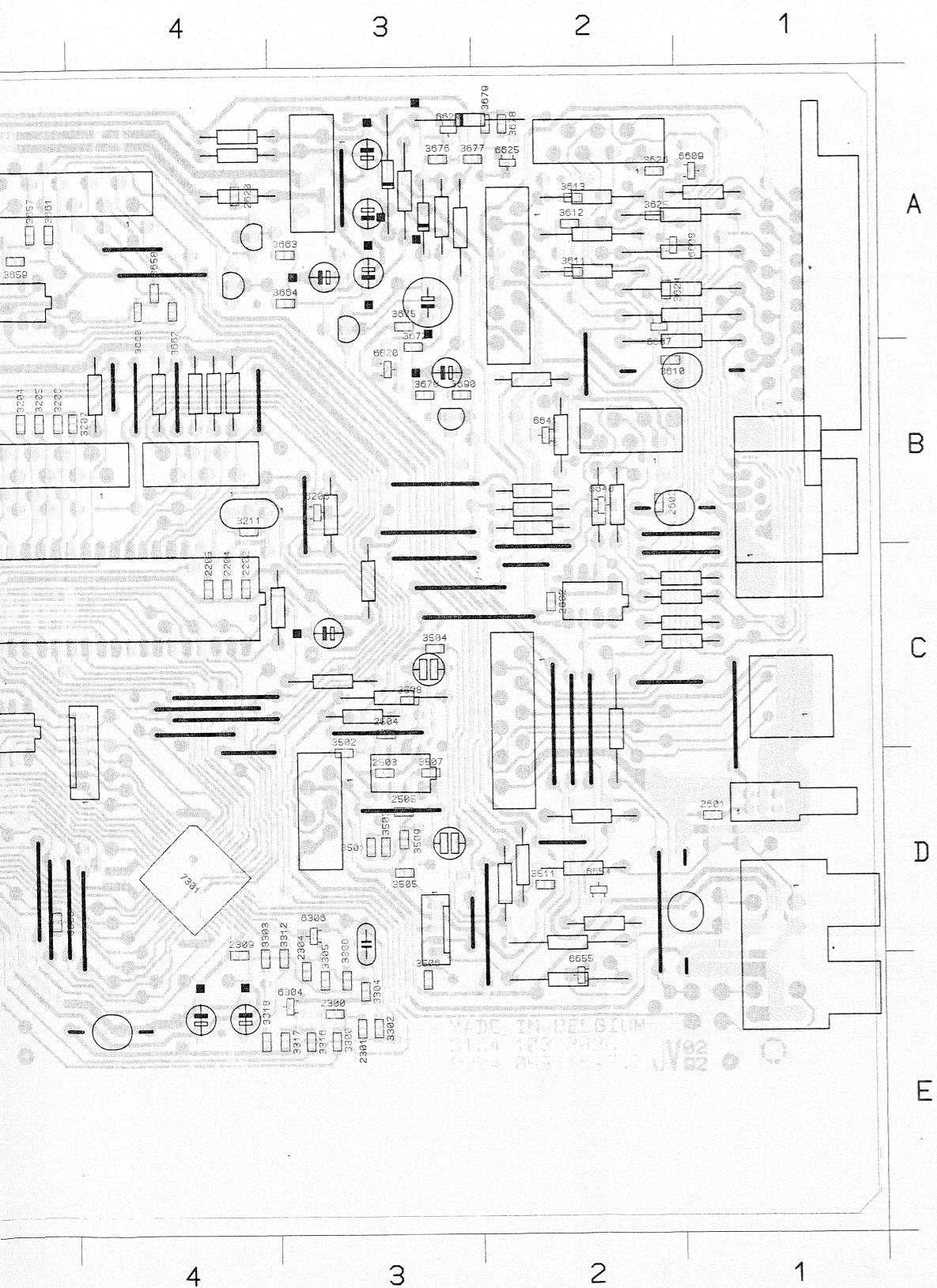
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0084 B 6	0041 C 5	0020 B 3	0020 B 3	0302 D 6	0323 A 3	0103 B 7	3073 A 3	3043 A 1	3018 A 6	3324 D 3	3241 B 4	3211 B 4	3186 A 8	3165 A 7	3130 E 7	2104 B 7	2321 C 6	2205 C 4	2141 D 9	2106 C 7	15 B 4
0085 B 6	0042 C 7	0021 A 4	0021 A 4	0310 D 5	0324 A 3	0104 A 8	3074 A 7	3051 D 2	3019 A 6	3325 E 3	3242 B 4	3212 B 4	3187 A 8	3166 A 7	3140 D 8	2105 C 8	2322 D 6	2230 B 6	2142 D 9	2107 D 7	22 E 6
0086 B 6	0043 C 5	0022 A 7	0022 A 7	0315 D 3	0325 A 2	0105 A 7	3075 A 3	3052 D 2	3020 A 4	3326 D 3	3243 B 4	3213 B 4	3188 A 8	3167 B 7	3141 E 8	2106 C 7	2501 D 3	2231 B 6	2143 E 9	2108 C 8	24 C 6
0087 B 6	0044 C 7	0023 C 8	0023 C 8	0316 A 5	0326 A 3	0106 A 8	3076 A 3	3053 D 2	3021 A 4	3327 C 3	3244 B 4	3214 B 4	3189 A 8	3168 B 7	3142 D 9	2107 C 8	2502 C 3	2232 B 6	2150 E 8	2109 C 8	25 A 3
0088 B 1	0045 C 7	0024 D 5	0024 D 5	0317 C 2	0327 A 2	0107 A 9	3077 A 2	3054 D 2	3022 A 4	3328 D 3	3245 B 4	3215 B 4	3190 B 8	3169 B 7	3143 E 9	2108 C 8	2503 D 3	2300 E 3	2151 B 8	2110 B 8	26 C 1
0089 C 1	0046 B 9	0025 E 5	0025 E 5	0318 B 9	0328 B 9	0108 A 8	3078 A 2	3055 A 5	3023 A 2	3329 C 3	3246 C 3	3216 C 3	3191 B 7	3170 B 7	3144 D 9	2109 C 8	2504 C 3	2301 E 3	2152 D 9	2111 C 8	27 A 9
0090 D 2	0047 A 5	0026 D 4	0026 D 4	0319 D 4	0329 D 4	0109 A 8	3079 A 2	3056 A 5	3024 A 2	3330 C 6	3247 B 6	3217 B 6	3192 A 9	3171 B 8	3145 E 9	2110 C 7	2505 D 3	2302 E 3	2153 D 9	2112 C 8	40 B 6
0091 D 2	0048 D 5	0027 C 4	0027 C 4	0320 A 4	0330 A 4	0170 A 9	3080 A 7	3057 A 5	3025 A 2	3331 D 2	3248 C 3	3218 C 3	3193 A 9	3172 B 8	3150 E 8	2111 B 6	2601 D 1	2304 E 3	2100 A 7	2113 B 8	41 A 6
0092 D 2	0049 B 9	0028 C 3	0028 C 3	0321 A 2	0331 A 4	0171 A 8	3081 A 7	3058 A 4	3026 D 2	3332 D 7	3249 B 6	3220 B 6	3194 A 7	3173 B 7	3152 D 9	2112 C 8	2602 B 2	2307 E 4	2101 B 7	2114 C 9	50 D 3



6.4.2 LIST OF ELECTRICAL PARTS CD PANEL

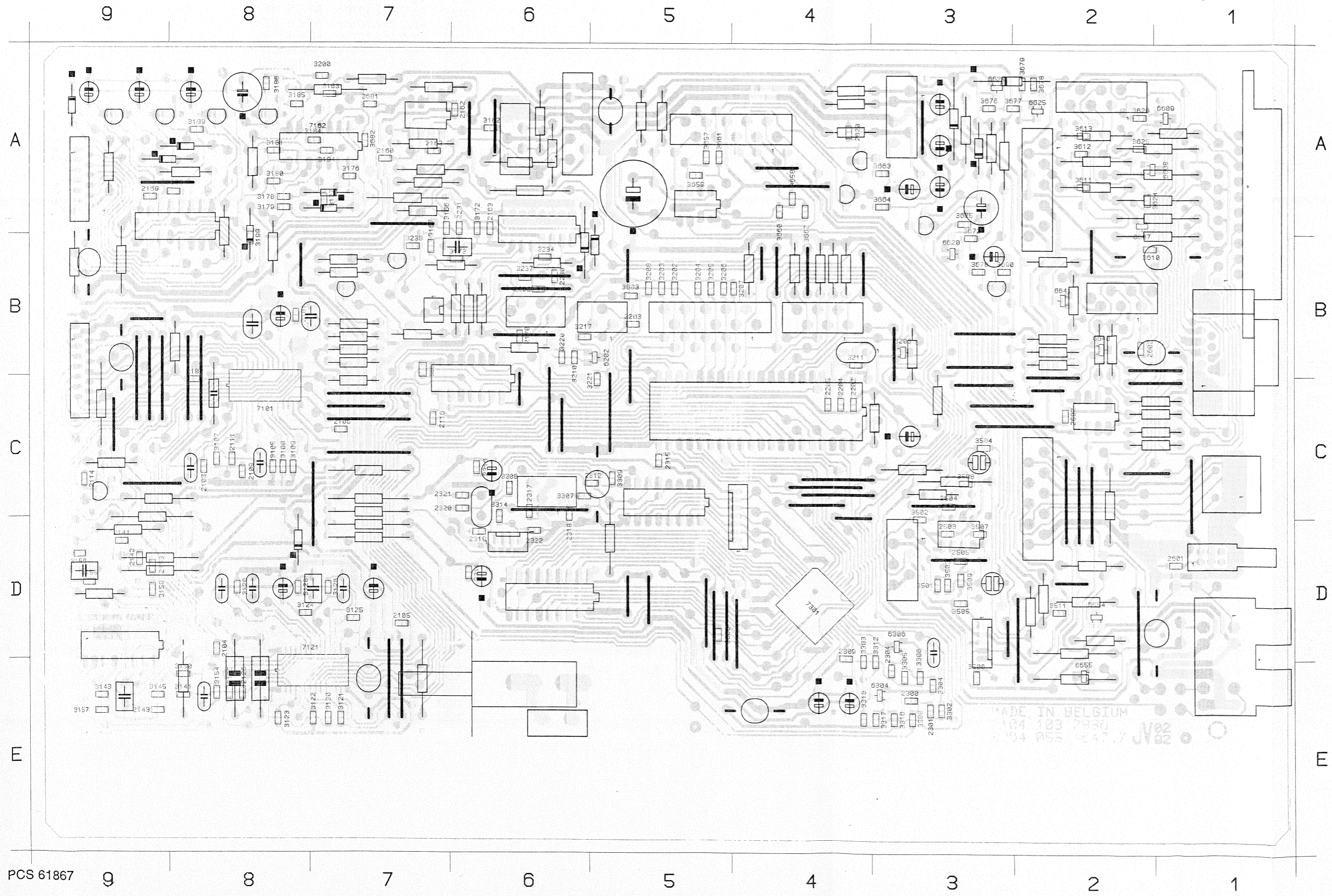
Item	Codenummer	Description
BU-6	4822 267 40857	CS7927-24-401
BU-7	4822 267 20414	CINCH SOCKET 4P
BU-8	4822 267 20414	CINCH SOCKET 4P
BU-9	4822 267 20414	CINCH SOCKET 4P
BU-10	4822 267 20414	CINCH SOCKET 4P
SK-1	4822 276 11309	MAINS-POWER SWITCH
1013	4822 267 60326	SCART CONN. 7087D
1201	4822 242 72527	CRYSTAL 4,000MHZ
3103	4822 052 10478	NFR25 4R7
3111	4822 052 10478	NFR25 4R7
3113	4822 052 10189	NFR25 18R
3114	4822 052 10129	NFR25 12R
3142	4822 052 10108	NFR25 1R0
3144	4822 052 10108	NFR25 1R0
3174	4822 052 10108	NFR25 1R0
3175	4822 052 10108	NFR25 1R0
3187	4822 052 10158	NFR25 1R5
3209	4822 052 10478	NFR25 4R7
3236	4822 052 10108	NFR25 1R0
3235	4822 052 10108	NFR25 1R0
3301	4822 052 10338	NFR25 3R3
3310	4822 052 10478	NFR25 4R7
3313	4822 052 10108	NFR25 1R0
3620	4822 052 10158	NFR25 1R5
3621	4822 052 10228	NFR25 2R2
3622	4822 052 10228	NFR25 2R2
3655	4822 052 10229	NFR25 22R
3656	4822 052 10229	NFR25 22R
3900	4822 052 10339	NFR25 33R PM5
6102	4822 130 44121	BC338
6161	5322 130 30684	1N4002
6162	4822 130 40941	BC558
6163	4822 130 40941	BC558
6203	4822 130 61207	BC848
6304	4822 130 61207	BC848
6306	4822 130 42131	BF550
6607	4822 130 61207	BC848
6608	4822 130 61207	BC848
6609	4822 130 61207	BC848
6620	4822 130 61207	BC848
6621	4822 130 40941	BC558
6622	5322 130 30684	1N4002
6623	4822 130 40941	BC558
6624	5322 130 41982	BC848B
6625	5322 130 41982	BC848B
6626	4822 130 30621	1N4148
6627	4822 130 30621	1N4148
6640	5322 130 41983	BC858B
6641	5322 130 41982	SMTRANS BC848B
6652	4822 130 40958	BC338-25
6653	4822 130 40958	BC338-25
6654	4822 130 42675	BC818
6655	4822 130 42675	BC818
7101	4822 209 73234	TDA8808T/C3
7121	4822 209 73235	TDA8809T/C2
7151	4822 209 72587	TCA0372DP2
7161	4822 209 83274	NJM4560D
7179	5322 209 11105	PC74HCT00P
7181	4822 209 72587	TCA0372DP2
7201	4822 209 30995	MC68HC05C8/SERVO PROC/2.1
7202	4822 209 70422	MN4264-15
7301	4822 209 61759	SAA7310GP/H5
7302	4822 209 70422	MN4264-15
7310	4822 209 62588	PCF3523P
7551	5322 209 86234	NE5532N
7651	4822 209 82362	NJM4556D
7681	4822 209 83163	LM833N

3221	C 5	3198	A 7	3174	A 7	3153	D 8	3114	B 9	2620	A 4	2386	E 4	2182	A 6	2115	B 8	51	D 4	1	A 6
3230	B 6	3199	B 8	3175	A 5	3154	E 8	3115	C 9	2621	A 3	2389	E 4	2183	B 6	2116	C 7	52	D 6	2	A 2
3231	B 6	3200	A 7	3176	A 7	3155	D 9	3120	D 8	2622	A 3	2310	D 6	2184	A 8	2120	E 8	61	A 2	3	B 4
3232	B 7	3202	B 5	3177	A 7	3156	D 9	3121	E 7	2623	A 3	2311	D 6	2185	A 9	2121	E 8	62	C 2	5	B 5
3233	B 6	3203	B 5	3178	A 8	3157	E 9	3122	E 7	2630	B 3	2312	C 6	2187	A 9	2122	D 8	1023	E 6	6	A 4
3234	B 6	3204	B 5	3179	A 8	3158	D 9	3123	E 8	2631	A 3	2314	C 6	2188	A 9	2123	D 7	1030	D 1	7	B 7
3235	A 7	3205	B 5	3180	A 8	3159	D 9	3124	D 8	2632	A 3	2315	C 5	2189	A 9	2124	D 7	1201	B 4	8	B 9
3236	A 6	3206	B 5	3181	A 8	3160	B 4	3125	D 7	2681	A 5	2316	C-6	2170	B 6	2125	E 8	2101	B 8	9	D 3
3237	B 6	3207	B 4	3182	A 8	3161	A 6	3126	D 7	2682	C 2	2317	D 5	2201	C 3	2126	E 8	2102	C 8	10	D 1
3238	B 7	3208	B 5	3183	A 7	3162	A 6	3127	D 7	3101	B 7	2318	D 6	2202	C 4	2127	D 8	2103	C 8	12	C 1
3300	E 3	3209	C 3	3184	A 7	3163	A 7	3128	D 8	3102	C 8	2319	D 6	2203	B 5	2128	D 8	2104	E 8	13	B 1
3301	D 7	3210	B 6	3185	A 8	3164	B 7	3129	B 8	3103	B 7	2320	C 6	2204	C 4	2140	E 9	2105	D 7	14	B 2
3302	E 3	3211	B 4	3186	A 8	3165	A 7	3130	E 7	3104	B 7	2321	C 6	2205	C 4	2141	D 9	2106	C 7	15	B 4
3303	E 4	3212	B 4	3187	A 8	3166	A 7	3140	D 8	3105	C 8	2322	D 6	2230	B 6	2142	D 9	2107	D 7	22	E 6
3304	E 3	3213	B 4	3188	A 8	3167	B 7	3141	E 8	3106	C 7	2501	D 3	2231	B 6	2143	E 9	2108	C 8	24	C 6
3305	E 3	3214	B 4	3189	A 8	3168	B 7	3142	D 9	3107	C 8	2502	C 3	2232	B 6	2150	E 8	2109	C 8	25	A 3
3306	E 3	3215	B 4	3190	A 8	3169	B 7	3143	D 9	3108	C 8	2503	D 3	2300	E 3	2151	B 8	2110	B 8	26	C 1
3307	C 5	3216	C 3	3191	B 9	3170	B 7	3144	D 9	3109	C 8	2504	C 3	2301	E 3	2152	D 0	2111	C 8	27	A 9
3308	C 6	3217	B 6	3192	A 9	3171	B 6	3145	E 9	3110	C 7	2505	D 3	2302	E 3	2153	D 0	2112	C 8	40	B 6
3309	C 5	3218	C 3	3193	A 9	3172	B 6	3146	E 8	3111	D 1	2601	D 1	2304	E 3	2150	A 7	2113	B 8	41	A 6
3310	D 7	3220	B 6	3194	A 7	3173	B 7	3152	D 9	3113	C 8	2602	B 2	2307	E 4	2151	B 7	2114	C 9	50	D 3

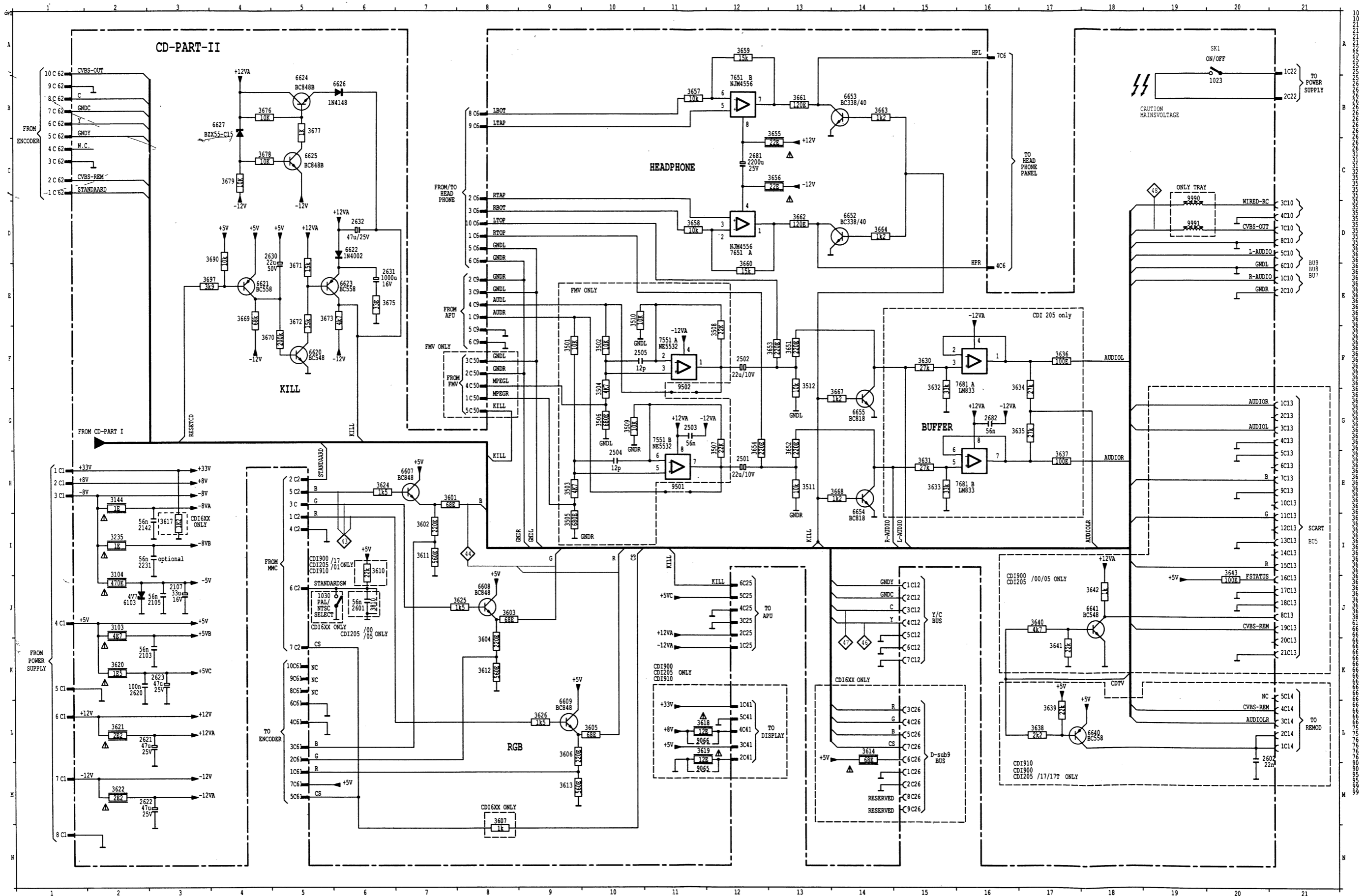


6.4.3 CD PANEL PCB, COPPER TRACK/SMD SIDE VIEW

0072 D 2	0050 B 9	0029 D 5	0007 D 5	6554 D 2	6172 A 8	3690 B 3	3650 A 5	3631 C 2	3602 A 2	3311 C 7	3221 C 5	3198 A 7	3174 A 7	3153 D 8	3114 B 9	2620 A 4	2308 E 4	2162 A 6	2115 B 8	51 D 4	1 A 6
0073 E 2	0051 E 7	0030 C 3	0008 B 8	6555 E 2	6173 A 8	3697 C 3	3650 A 4	3632 C 1	3603 A 2	3312 E 3	3230 B 6	3199 B 9	3175 A 6	3154 E 8	3115 C 9	2621 A 3	2309 E 4	2163 B 6	2116 C 7	52 D 6	2 A 2
0074 C 3	0052 D 2	0031 D 7	0009 A 6	7101 C 8	6202 B 5	3602 C 7	3661 A 5	3633 C 1	3604 A 2	3313 C 7	3231 B 6	3200 A 7	3176 A 7	3155 D 9	3120 D 8	2622 A 3	2310 D 6	2164 A 8	2120 E 8	61 A 2	3 B 4
0075 C 2	0053 B 2	0032 D 7	0011 D 5	7121 E 8	6203 B 3	3603 B 5	3662 A 4	3634 B 2	3605 A 2	3314 C 6	3232 B 7	3202 B 5	3177 A 7	3156 D 9	3121 E 7	2623 A 3	2311 D 6	2165 A 9	2121 E 8	62 C 2	5 B 5
0076 C 2	0054 B 1	0033 B 9	0012 B 5	7151 E 9	6304 E 3	3606 A 9	3663 A 3	3635 C 2	3606 A 2	3316 E 3	3233 B 6	3203 B 5	3178 A 8	3157 E 9	3122 E 7	2630 B 3	2312 C 6	2167 A 9	2122 D 8	1023 E 6	6 A 4
0077 D 3	0055 C 1	0034 B 9	0013 A 8	7161 A 7	6308 D 3	3608 D 5	3664 A 3	3636 C 1	3607 A 1	3317 E 3	3234 B 6	3204 B 5	3179 A 8	3158 D 9	3123 E 8	2631 A 3	2314 C 6	2168 A 8	2123 D 7	1030 D 1	7 B 7
0078 C 2	0056 B 4	0035 B 3	0014 B 3	7162 A 7	6607 A 7	5301 D 6	3607 E 2	3637 C 1	3610 B 2	3318 E 4	3235 A 7	3205 B 5	3180 A 8	3159 D 9	3124 D 8	2632 A 3	2315 C 5	2169 A 9	2124 D 7	1201 B 4	8 B 9
0079 A 3	0057 B 4	0036 C 2	0015 C 6	7164 B 8	6608 A 2	6102 C 9	3608 D 2	3638 B 2	3611 A 2	3319 D 5	3236 A 6	3206 B 5	3181 A 8	3160 B 4	3125 D 7	2681 A 5	2316 C 6	2170 B 6	2125 E 8	1201 B 8	9 D 3
0080 C 6	0058 B 4	0037 B 8	0016 C 9	7179 C 6	6609 A 1	6103 D 8	3609 A 3	3639 B 2	3612 A 2	3321 D 3	3237 B 6	3207 B 4	3182 A 8	3161 A 6	3126 D 7	2682 C 2	2317 D 6	2201 C 3	2126 E 8	2102 C 9	10 D 1
0081 A 6	0059 B 6	0038 B 8	0017 C 4	7181 B 6	6620 B 3	6104 A 6	3670 B 3	3640 B 2	3613 A 2	3322 D 3	3238 B 7	3208 B 5	3183 A 7	3162 A 6	3127 D 7	3101 B 7	2318 D 6	2202 C 4	2127 D 8	2103 C 8	12 C 1
9501 D 3	0061 C 1	0039 D 2	0018 C 7	7201 C 4	6621 B 3	6101 B 5	3671 A 3	3641 B 2	3614 B 2	3323 D 3	3200 C 3	3209 C 3	3184 A 7	3163 A 7	3128 D 8	3102 C 8	2319 D 6	2203 B 5	2128 D 8	2104 E 8	13 B 1
9502 C 3	0062 B 4	0040 C 7	0019 E 5	7301 D 4	6622 A 3	6102 B 7	3672 B 3	3642 B 2	3617 A 6	3324 C 3	3201 D 7	3210 B 6	3185 A 8	3164 B 7	3129 B 8	3103 B 7	2320 C 6	2204 C 4	2140 E 9	2105 D 7	14 B 2
	0063 C 6	0041 C 5	0020 B 3	7302 D 6	6623 A 3	6103 B 7	3673 A 3	3643 A 1	3618 A 6	3325 D 3	3202 E 3	3211 B 4	3186 A 8	3165 A 7	3130 E 7	3104 B 7	2321 C 6	2205 C 4	2141 D 9	2106 C 7	15 B 4
	0064 B 6	0042 C 7	0021 A 4	7310 D 5	6624 A 3	6104 A 8	3674 A 7	3651 D 2	3619 A 6	3326 E 3	3203 E 4	3212 B 4	3187 A 8	3166 A 7	3140 D 8	3105 C 8	2322 D 6	2230 B 6	2142 D 9	2107 D 7	22 E 6
	0065 B 6	0043 C 5	0022 A 7	7551 D 3	6625 A 2	6105 A 7	3675 A 3	3652 D 2	3620 A 4	3327 D 3	3204 E 3	3213 B 4	3188 A 8	3167 B 7	3141 E 8	3106 C 7	2501 D 3	2231 B 6	2143 E 9	2108 C 8	24 C 6
	0066 B 6	0044 C 7	0023 C 8	7651 A 5	6626 A 3	6106 A 8	3676 A 3	3653 D 2	3621 A 4	3328 C 3	3205 E 3	3214 B 4	3189 A 8	3168 B 7	3142 D 9	3107 C 8	2502 C 3	2232 B 6	2150 E 8	2109 C 8	25 A 3
	0067 C 1	0045 C 7	0024 D 5	7681 C 2	6627 A 2	6107 A 9	3677 A 2	3654 D 2	3622 A 4	3329 D 3	3206 E 3	3215 B 4	3190 B 8	3169 B 7	3143 E 9	3108 C 8	2503 D 3	2300 E 3	2151 B 8	2110 B 8	26 C 1
	0068 C 1	0046 B 9	0025 E 5	9002 B 9	6640 B 2	6108 A 8	3678 A 2	3655 A 5	3624 A 2	3330 C 3	3207 C 5	3216 C 3	3191 B 9	3170 B 7	3144 D 9	3109 C 8	2504 C 3	2301 E 3	2152 D 9	2111 C 8	27 A 9
	0069 D 2	0047 A 5	0026 D 4	9003 D 4	6641 B 2	6109 A 8	3679 A 2	3656 A 5	3625 A 2	3331 D 2	3208 C 6	3217 B 6	3192 A 9	3171 B 6	3145 E 9	3110 C 7	2505 D 3	2302 E 3	2153 D 9	2112 C 8	40 B 6
	0070 D 2	0048 D 5	0027 C 4	9005 A 4	6652 A 4	6170 A 0	3681 A 7	3657 A 5	3626 A 2	3332 C 3	3209 C 5	3218 C 3	3193 A 9	3172 B 6	3150 E 8	3111 B 6	2601 D 1	2304 E 3	2180 A 7	2113 B 8	41 A 6
	0071 D 2	0049 B 9	0028 C 3	9006 A 2	6653 A 4	6171 A 8	3682 A 7	3658 A 4	3630 D 2	3333 D 7	3210 B 6	3220 B 6	3194 A 7	3173 B 7	3152 D 9	3113 C 8	2602 B 2	2307 E 4	2181 B 7	2114 C 9	50 D 3

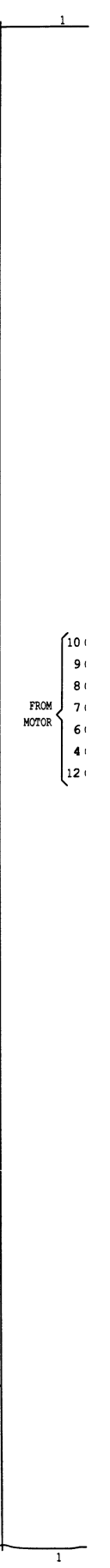


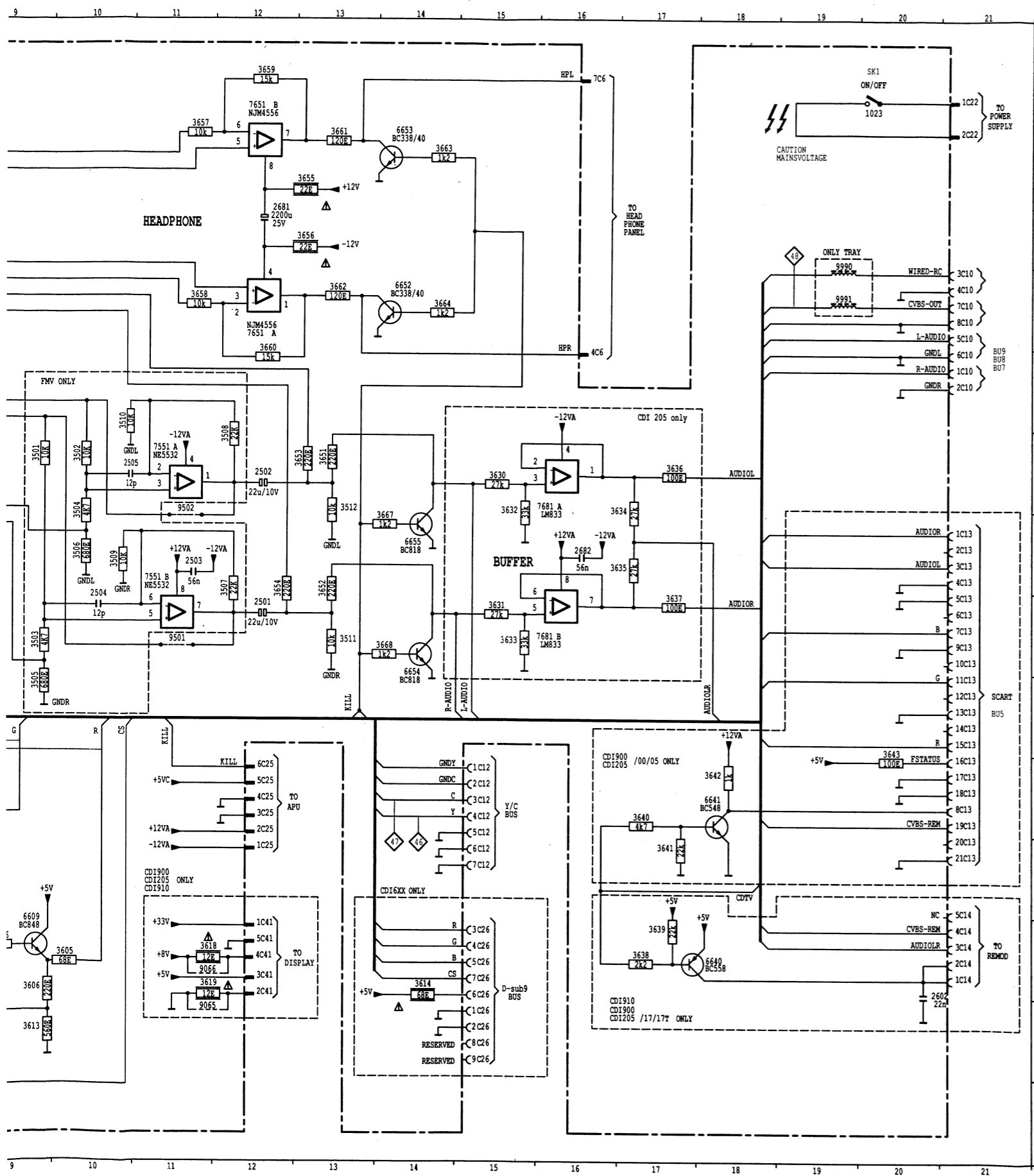
6.4.4 CIRCUIT DIAGRAM CD PART 2



6.4.5 CIR THIS CIR

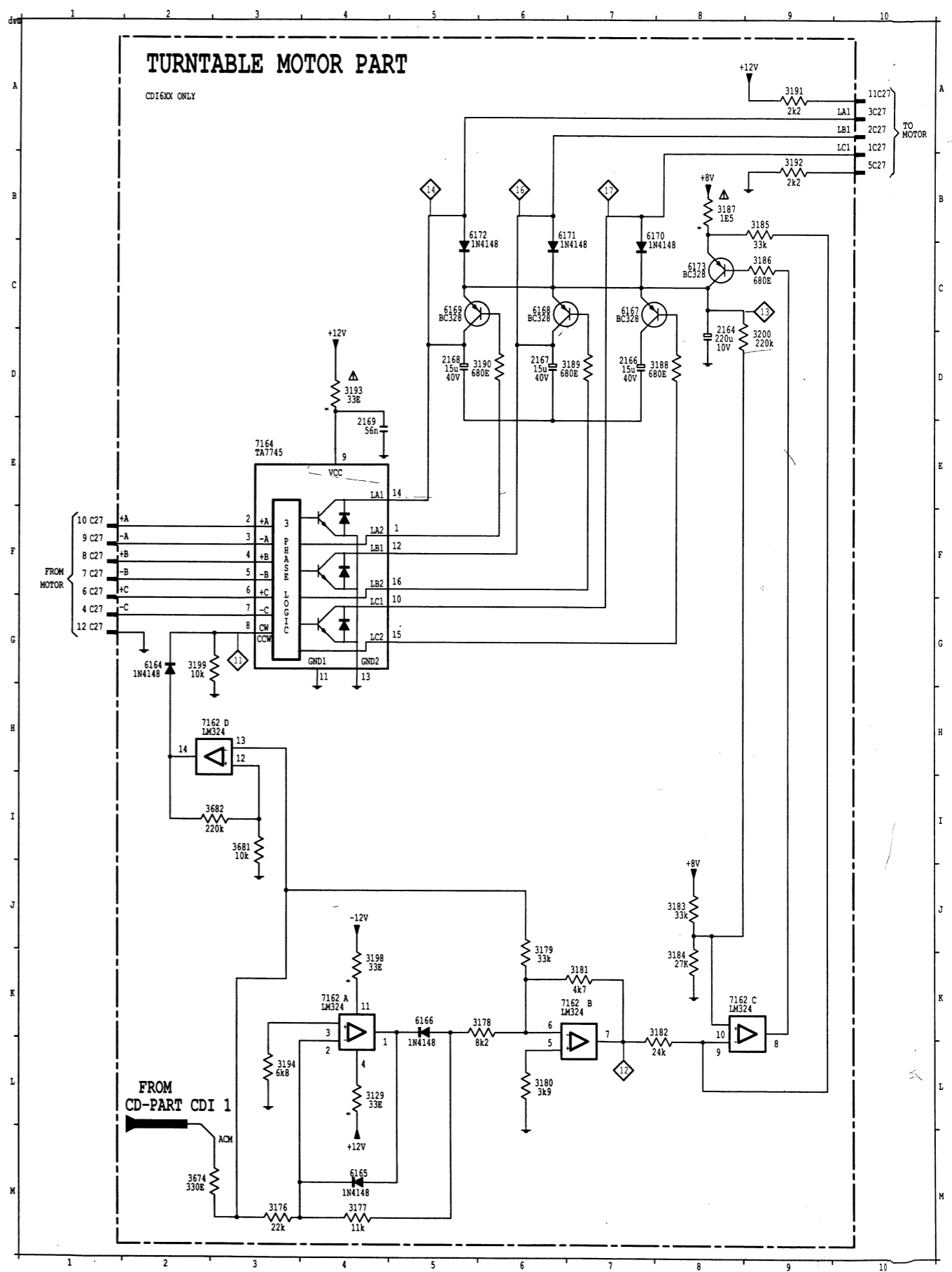
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2166	D	7	312
2167	D	6	317
2168	D	5	317



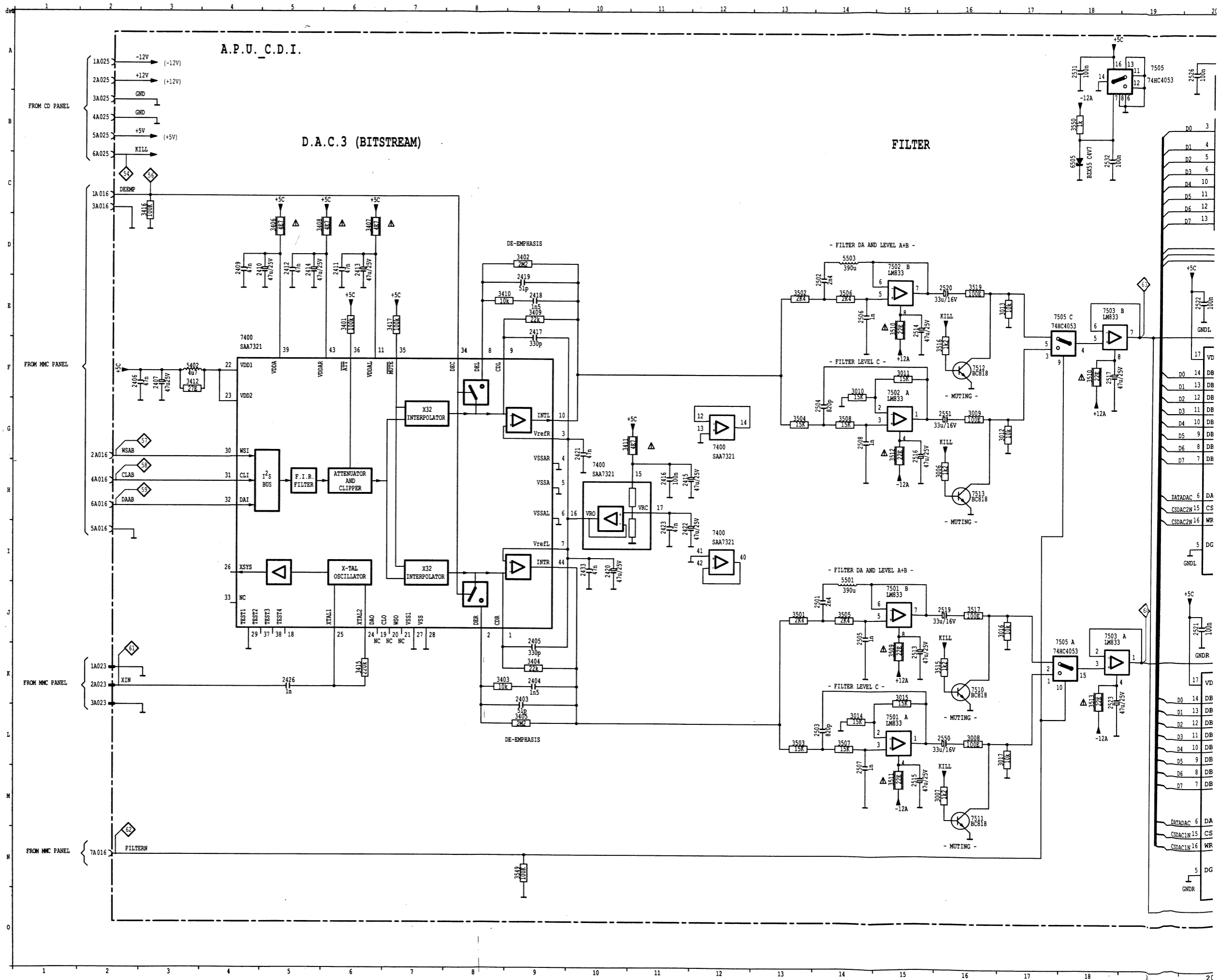


6.4.5. CIRCUIT DIAGRAM TURNTABLE MOTOR PART
THIS CIRCUIT IS NOT RELEVANT FOR CDI205

2164	C 8	2169	E 4	3178	K 6	3182	K 8	3186	D 9	3190	D 6	3194	L 3	3674	M 2	6165	M 4	6169	C 5	6173	C 8	7162	L 3	7164	L 4	C 27	F 1	C 27	F 1	C 27	A10
2186	D 5	3176	M 4	3179	L 6	3183	K 8	3187	D 9	3191	D 6	3195	L 3	3683	M 2	6166	M 4	6170	C 5	6174	C 8	7162	L 3	7164	L 4	C 27	F 1	C 27	F 1	C 27	A10
2187	D 5	3177	M 4	3180	L 6	3184	K 8	3188	D 9	3192	D 6	3196	L 3	3684	M 2	6167	M 4	6171	C 5	6175	C 8	7162	L 3	7164	L 4	C 27	F 1	C 27	F 1	C 27	A10

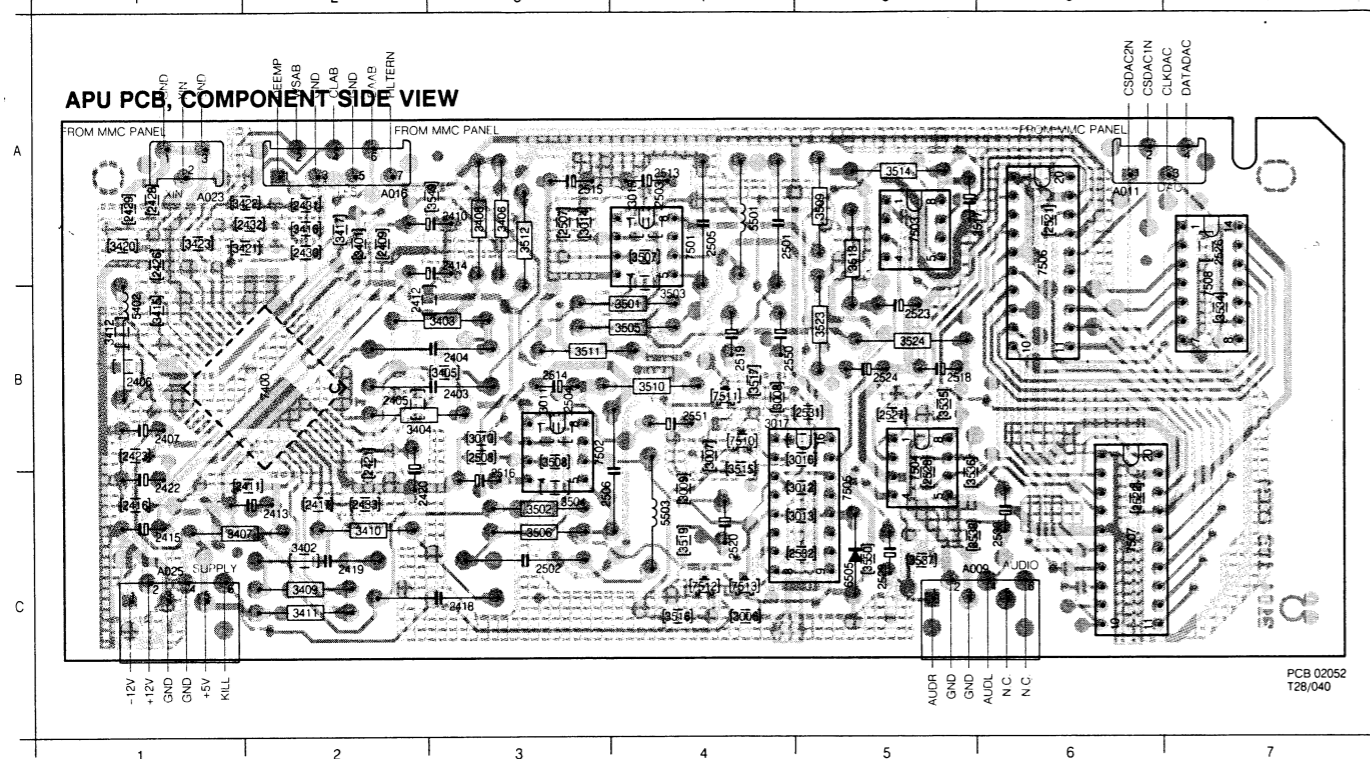


6.5.1 APU CIRCUIT DIAGRAM

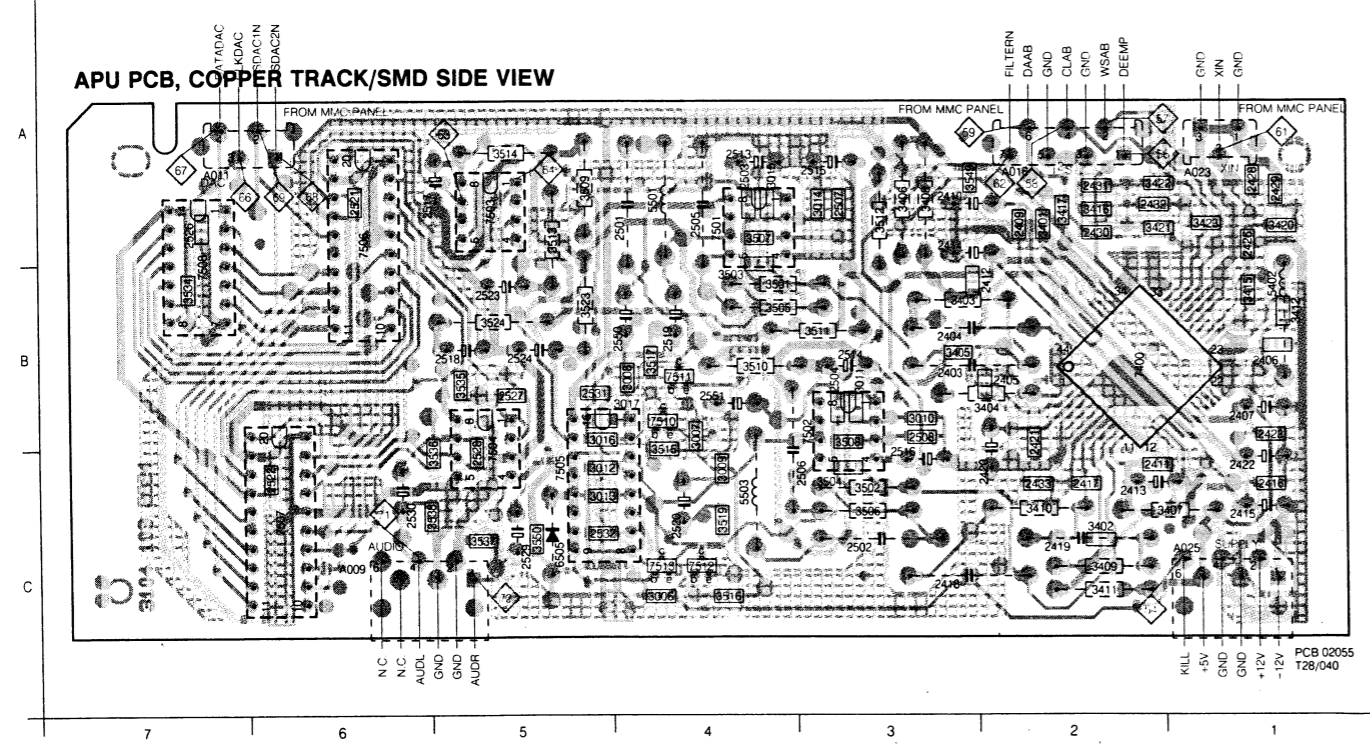


6.5.2 APU PCB, COMPONENT SIDE VIEW AND COPPER TRACK/SMD SIDE VIEW

2403 B3	2415 C1	2429 A1	2507 A3	2522 C6	2551 B4	3016 B4	3410 C2	3502 C3	3513 A5	3537 C5	7503 A5	A011 A6
2404 B3	2416 C1	2430 A2	2508 B3	2523 B5	3006 C4	3017 B4	3411 C2	3503 B4	3514 A5	3538 C6	7504 C5	A016 A2
2405 B2	2417 C2	2431 A2	2513 A4	2524 B5	3007 B4	3401 A2	3412 B1	3504 C3	3515 C4	3549 A3	7505 C5	A023 A1
2406 B1	2418 C3	2432 A1	2514 B3	2526 A7	3008 B4	3402 C2	3415 B1	3505 B4	3516 C4	3550 C5	7506 A6	A025 C1
2407 B1	2419 C2	2433 C2	2515 A3	2527 B5	3009 C4	3403 B3	3416 A2	3506 C3	3517 B4	5402 B1	7507 C6	
2409 A2	2420 C3	2501 A4	2516 C3	2528 C5	3010 B3	3404 B2	3417 A2	3507 A4	3519 C4	5501 A4	7508 B7	
2410 A3	2421 C3	2502 C3	2517 A6	2529 C5	3011 B3	3405 B3	3420 A1	3508 B3	3523 B5	5503 C4	7510 B4	
2411 C1	2422 C1	2503 A4	2518 B5	2530 C6	3012 C4	3406 A3	3421 A1	3509 A5	3524 B5	6505 C5	7511 B4	
2412 B2	2423 B1	2504 B3	2519 B4	2531 B5	3013 C4	3407 C1	3422 A1	3510 B4	3534 B7	7400 B2	7512 C4	
2413 C2	2426 A1	2505 A4	2520 C4	2532 C4	3014 A3	3408 A3	3423 A1	3511 B3	3535 B5	7501 A4	7513 C4	
2414 A3	2428 A1	2506 C4	2521 A6	2550 B4	3015 A4	3409 C2	3501 B4	3512 A3	3536 C6	7502 B3	A009 C5	



2403 B3	2415 C1	2429 A1	2507 A3	2522 C6	2551 B4	3016 B4	3410 C2	3502 C3	3513 A5	3537 C5	7503 A5	A011 A6
2404 B3	2416 C1	2430 A2	2508 B3	2523 B5	3006 C4	3017 B4	3411 C2	3503 B4	3514 A5	3538 C6	7504 C5	A016 A2
2405 B2	2417 C2	2431 A2	2513 A4	2524 B5	3007 B4	3401 A2	3412 B1	3504 C3	3515 C4	3549 A3	7505 C5	A023 A1
2406 B1	2418 C3	2432 A1	2514 B3	2526 A7	3008 B4	3402 C2	3415 B1	3505 B4	3516 C4	3550 C5	7506 A6	A025 C1
2407 B1	2419 C2	2433 C2	2515 A3	2527 B5	3009 C4	3403 B3	3416 A2	3506 C3	3517 B4	5402 B1	7507 C6	
2409 A2	2420 C3	2501 A4	2516 C3	2528 C5	3010 B3	3404 B2	3417 A2	3507 A4	3519 C4	5501 A4	7508 B7	
2410 A3	2421 C3	2502 C3	2517 A6	2529 C5	3011 B3	3405 B3	3420 A1	3508 B3	3523 B5	5503 C4	7510 B4	
2411 C1	2422 C1	2503 A4	2518 B5	2530 C6	3012 C4	3406 A3	3421 A1	3509 A5	3524 B5	6505 C5	7511 B4	
2412 B2	2423 B1	2504 B3	2519 B4	2531 B5	3013 C4	3407 C1	3422 A1	3510 B4	3534 B7	7400 B2	7512 C4	
2413 C2	2426 A1	2505 A4	2520 C4	2532 C4	3014 A3	3408 A3	3423 A1	3511 B3	3535 B5	7501 A4	7513 C4	
2414 A3	2428 A1	2506 C4	2521 A6	2550 B4	3015 A4	3409 C2	3501 B4	3512 A3	3536 C6	7502 B3	A009 C5	

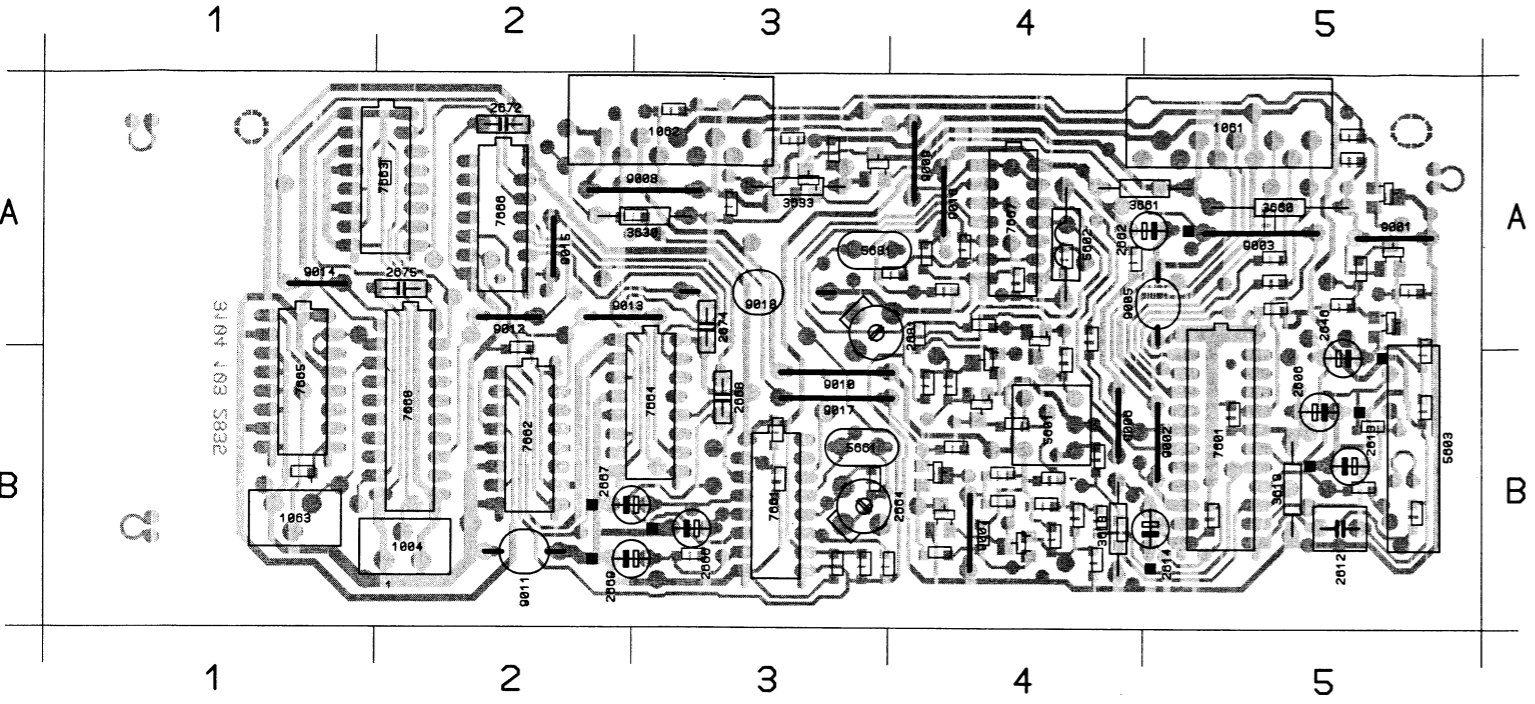


6.5.3 LIST OF ELECTRICAL PARTS APU

Item	Codenumber	Description
2529	4822 124 41738	BIP. 22MU10V
2530	4822 124 41738	BIP. 22MU10V
3406	4822 052 10478	NFR25 4R7
3407	4822 052 10478	NFR25 4R7
3408	4822 052 10478	NFR25 4R7
3411	4822 052 10478	NFR25 4R7
3509	4822 052 10229	NFR25 22R
3510	4822 052 10229	NFR25 22R
3511	4822 052 10229	NFR25 22R
3512	4822 052 10229	NFR25 22R
3513	4822 052 10229	NFR25 22R
3514	4822 052 10229	NFR25 22R
3523	4822 052 10229	NFR25 22R
6505	4822 130 34174	BZX55-C4V7
7400	4822 209 61708	SAA7321GP
7501	4822 209 83163	LM833N
7502	4822 209 83163	LM833N
7503	4822 209 83163	LM833N
7504	4822 209 83163	LM833N
7505	4822 209 71584	74HCT4053P
7506	4822 209 63496	AD7528JN
7507	4822 209 63496	AD7528JN
7508	5322 209 11268	74HCT164P
7510	4822 130 42675	BC818
7511	4822 130 42675	BC818
7512	4822 130 42675	BC818
7512	4822 130 42675	BC818

6.6.1 VIDEO ENCODER PCB, COMPONENT SIDE VIEW

1004 B 2	2000 B 5	2015 B 5	2002 A 4	2070 A 4	2082 A 4	3018 B 4	3030 A 3	3038 B 4	3000 A 5	3083 A 4	7001 A 5	7040 B 4	7005 A 1	0000 B 4	0014 A 1
1001 A 5	2007 B 4	2041 B 4	2003 B 3	2071 A 2	2083 A 4	3010 B 5	3031 B 5	3039 B 4	3001 A 5	3084 A 4	7002 A 4	7041 B 4	7006 A 2	0007 B 4	0015 A 2
1002 A 3	2009 A 5	2042 B 4	2004 B 3	2072 A 2	2082 B 5	3024 A 3	3032 A 3	3040 B 4	3002 B 3	3700 A 5	7004 B 4	7042 A 3	7007 A 4	0008 A 2	0016 A 4
1003 B 1	2010 A 5	2043 B 4	2005 B 3	2073 B 2	2083 B 5	3025 B 5	3033 A 3	3041 A 4	3003 B 3	5001 B 4	7020 A 5	7043 A 3	7008 A 2	0009 A 4	0017 B 4
2002 A 4	2011 A 5	2044 B 4	2006 B 3	2074 A 3	2084 B 4	3026 A 3	3034 A 3	3042 B 4	3004 B 3	5002 A 4	7027 B 4	7001 B 3	0001 A 5	0010 B 4	0018 A 3
2003 B 5	2012 B 5	2045 A 5	2007 B 3	2075 A 2	2085 B 4	3027 A 5	3035 A 5	3043 B 4	3005 B 3	5003 B 5	7028 A 5	7002 B 2	0002 B 5	0011 B 2	
2004 B 4	2013 B 5	2046 B 5	2008 B 3	2076 B 1	2087 A 5	3028 A 3	3036 A 5	3044 B 4	3006 B 4	5004 A 5	7029 A 5	7003 A 1	0003 A 5	0012 A 2	
2005 B 4	2014 B 5	2001 B 3	2009 B 3	2081 A 3	2088 B 5	3029 B 4	3037 B 4	3045 B 4	3007 A 4	5005 B 3	7030 B 4	7004 A 2	0005 A 5	0013 A 3	

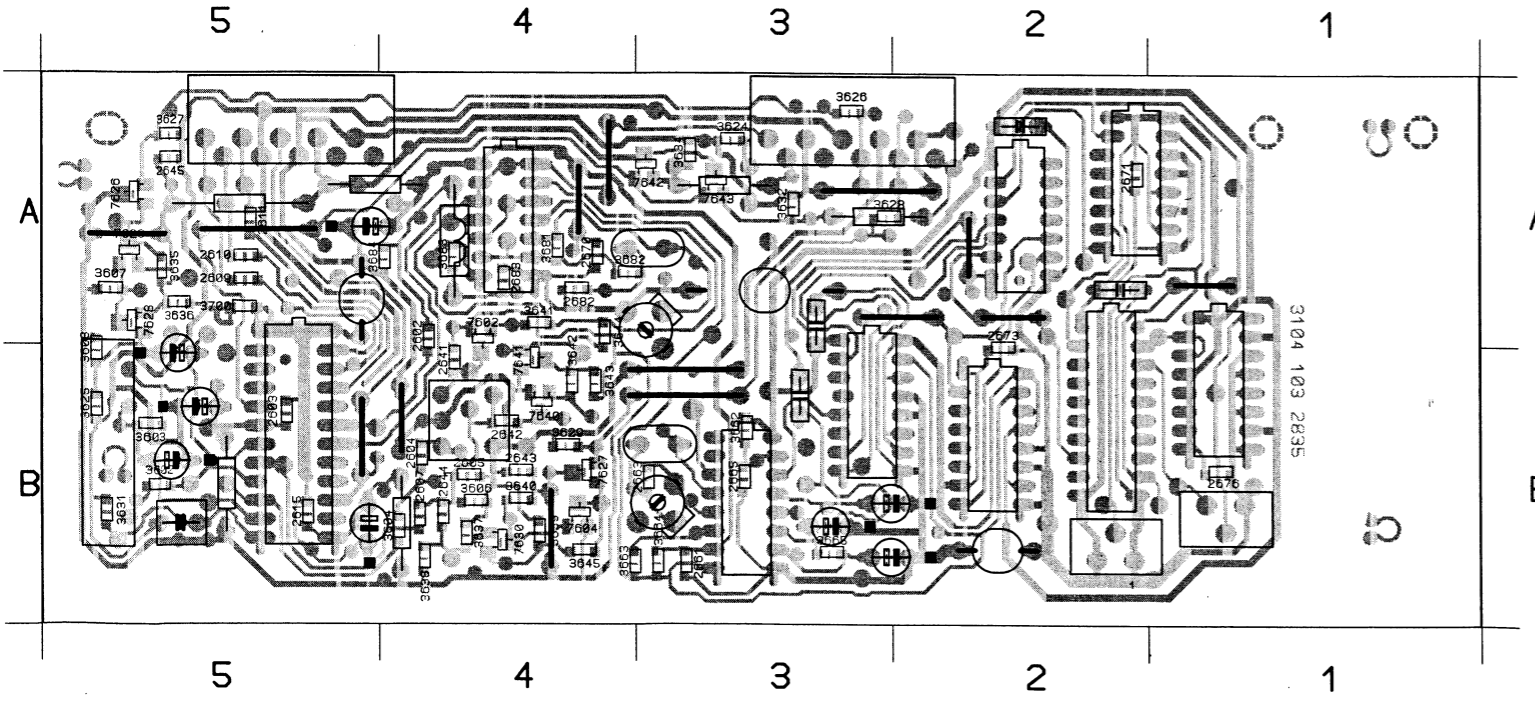


6.6.2 LIST OF ELECTRICAL PARTS VIDEO ENCODER

Item	Codenummer	Description
2681	4822 125 50045	TRIM 1P8-22P
3618	4822 052 10228	NFR25 2R2
3619	4822 052 10228	NFR25 2R2
3660	4822 052 10108	NFR25 1R0
3661	4822 052 10108	NFR25 1R0
5681	4822 242 70933	X-TAL 4MHZ433
7601	4822 209 63497	CXA1145P
7604	5322 130 41983	BC858BT
7626	4822 130 61207	BC848
7627	4822 130 61207	BC848
7628	4822 130 61207	BC848
7629	5322 130 41983	BC858BT
7630	4822 130 61207	BC848
7642	4822 130 61207	BC848
7643	4822 130 61207	BC848
7667	5322 209 83218	PC74HC00P

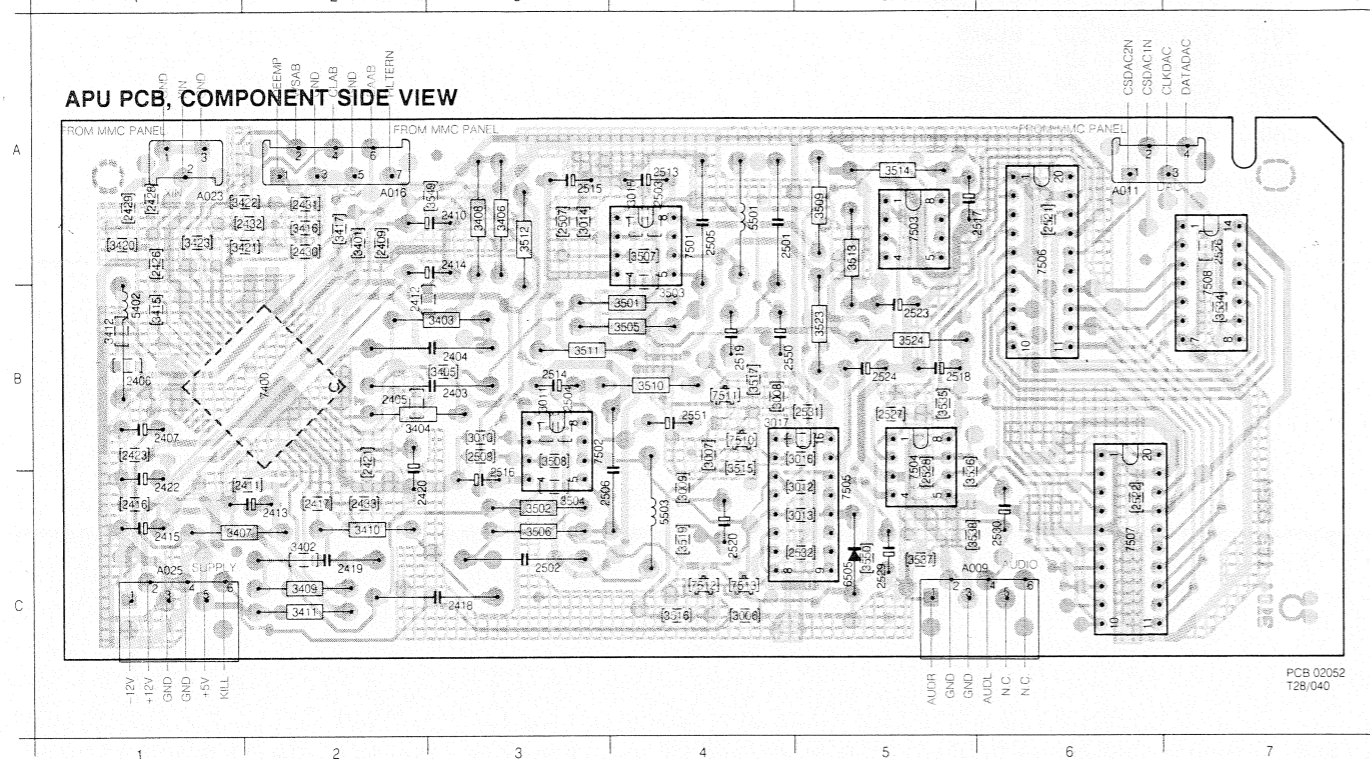
6.6.1 VIDEO ENCODER PCB, COPPER TRACK/SMD SIDE VIEW

0014 A 1	0000 B 4	7005 A 1	7040 B 4	7001 A 5	3083 A 4	3000 A 5	3038 B 4	3030 A 3	3018 B 4	2082 A 4	2070 A 4	2002 A 4	2015 B 5	2000 B 5	1004 B 2
0015 A 2	0007 B 4	7006 A 2	7041 B 4	7002 A 4	3084 A 4	3001 A 5	3039 B 4	3031 B 5	3010 B 5	2083 A 4	2071 A 2	2003 B 3	2041 B 4	2007 B 4	1001 A 5
0016 A 4	0009 A 2	7007 A 4	7042 A 3	7004 B 4	3700 A 5	3002 B 3	3040 B 4	3032 A 3	3024 A 3	3002 B 5	2072 A 2	2004 B 3	2042 B 4	2009 A 5	1002 A 3
0017 B 4	0000 A 4	7008 A 2	7043 A 3	7020 A 5	5001 B 4	3033 A 3	3041 A 4	3033 A 3	3025 B 5	3003 B 5	2073 B 2	2005 B 3	2043 B 4	2010 A 5	1003 B 1
0018 A 3	0010 B 4	0001 A 5	7001 B 3	7027 B 4	5002 A 4	3004 B 3	3042 B 4	3034 A 3	3026 A 3	3004 B 4	2074 A 3	2006 B 3	2044 B 4	2011 A 5	2002 A 4
0011 B 2	0002 B 5	7002 B 2	7028 A 5	5003 B 5	3005 B 3	3043 B 4	3035 A 5	3027 A 5	3006 B 4	2075 A 2	2007 B 3	2045 A 5	2012 B 5	2003 B 5	
0012 A 2	0003 A 5	7003 A 1	7029 A 5	5001 B 3	3081 A 4	3044 A 4	3036 A 5	3028 A 3	3007 A 5	2076 B 1	2008 B 3	2046 B 5	2013 B 5	2004 B 4	
0013 A 3	0005 A 5	7004 A 2	7030 B 4	5001 A 4	3082 A 4	3045 B 4	3037 B 4	3029 B 4	3008 B 5	2081 A 3	2009 B 3	2001 B 3	2014 B 5	2005 B 4	

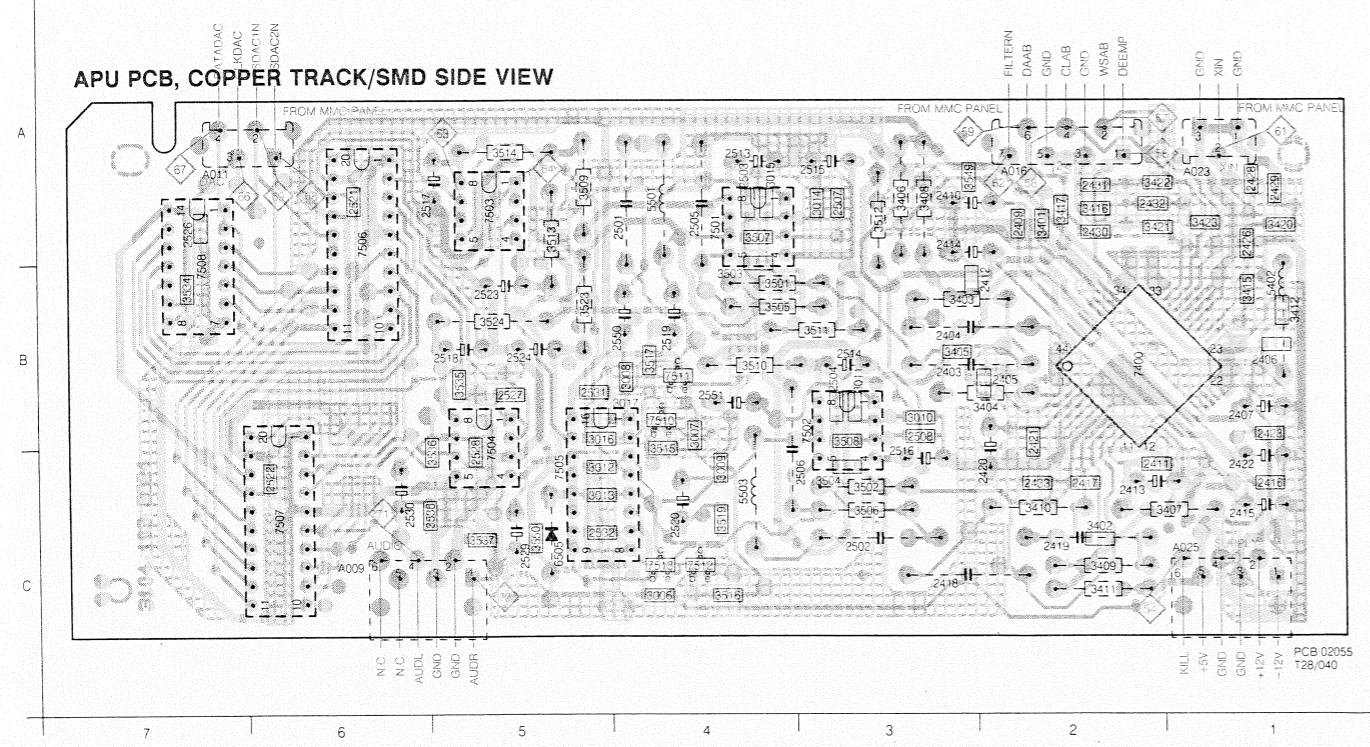


6.5.2 APU PCB, COMPONENT SIDE VIEW AND COPPER TRACK/SMD SIDE VIEW

2403 B3	2415 C1	2429 A1	2507 A3	2522 C6	2551 B4	3016 B4	3410 C2	3502 C3	3513 A5	3537 C5	7503 A5	A011 A6
2404 B3	2416 C1	2430 A2	2508 B3	2523 B5	3006 C4	3017 B4	3411 C2	3503 B4	3514 A5	3538 C6	7504 C5	A016 A2
2405 B2	2417 C2	2431 A2	2513 A4	2524 B5	3007 B4	3401 A2	3412 B1	3504 C3	3515 C4	3549 A3	7505 C5	A023 A1
2406 B1	2418 C3	2432 A1	2514 B3	2525 A7	3008 B4	3402 C2	3413 B1	3505 B4	3516 C4	3550 C5	7506 A6	A025 C1
2407 B1	2419 C3	2433 C2	2515 A3	2527 B5	3009 C4	3403 B3	3415 A2	3506 C3	3517 B1	3542 B1	7507 C6	
2409 A2	2420 C2	2501 A4	2516 C3	2528 C5	3010 B3	3404 B2	3417 A2	3507 A4	3519 C4	3501 A4	7508 B7	
2410 A3	2421 C3	2502 C3	2517 A6	2529 C5	3011 B3	3405 B3	3420 A1	3508 B3	3523 B5	5503 C4	7510 B4	
2411 C1	2422 C1	2503 A4	2518 B5	2530 C6	3012 C4	3406 A3	3421 A1	3509 A5	3524 B5	5505 C5	7511 B4	
2412 B2	2423 B1	2504 B3	2519 B4	2531 B5	3013 C4	3407 C1	3422 A1	3510 B4	3534 B7	7400 B2	7512 C4	
2413 C2	2424 A1	2505 A4	2520 C4	2532 C4	3014 A3	3408 A3	3423 A1	3511 B3	3535 B5	7501 A4	7513 C4	
2414 A3	2425 A1	2506 C4	2521 A6	2550 B4	3015 A4	3409 C2	3501 B4	3512 A3	3536 C6	7502 B3	A009 C5	



2403 B3	2415 C1	2429 A1	2507 A3	2522 C6	2551 B4	3016 B4	3410 C2	3502 C3	3513 A5	3537 C5	7503 A5	A011 A6
2404 B3	2416 C1	2430 A2	2508 B3	2523 B5	3006 C4	3017 B4	3411 C2	3503 B4	3514 A5	3538 C6	7504 C5	A016 A2
2405 B2	2417 C2	2431 A2	2513 A4	2524 B5	3007 B4	3401 A2	3412 B1	3504 C3	3515 C4	3549 A3	7505 C5	A023 A1
2406 B1	2418 C3	2432 A1	2514 B3	2525 A7	3008 B4	3402 C2	3413 B1	3505 B4	3516 C4	3550 C5	7506 A6	A025 C1
2407 B1	2419 C3	2433 C2	2515 A3	2527 B5	3009 C4	3403 B3	3415 A2	3506 C3	3517 B1	3542 B1	7507 C6	
2409 A2	2420 C2	2501 A4	2516 C3	2528 C5	3010 B3	3404 B2	3417 A2	3507 A4	3519 C4	3501 A4	7508 B7	
2410 A3	2421 C3	2502 C3	2517 A6	2529 C5	3011 B3	3405 B3	3420 A1	3508 B3	3523 B5	5503 C4	7510 B4	
2411 C1	2422 C1	2503 A4	2518 B5	2530 C6	3012 C4	3406 A3	3421 A1	3509 A5	3524 B5	5505 C5	7511 B4	
2412 B2	2423 B1	2504 B3	2519 B4	2531 B5	3013 C4	3407 C1	3422 A1	3510 B4	3534 B7	7400 B2	7512 C4	
2413 C2	2424 A1	2505 A4	2520 C4	2532 C4	3014 A3	3408 A3	3423 A1	3511 B3	3535 B5	7501 A4	7513 C4	
2414 A3	2425 A1	2506 C4	2521 A6	2550 B4	3015 A4	3409 C2	3501 B4	3512 A3	3536 C6	7502 B3	A009 C5	

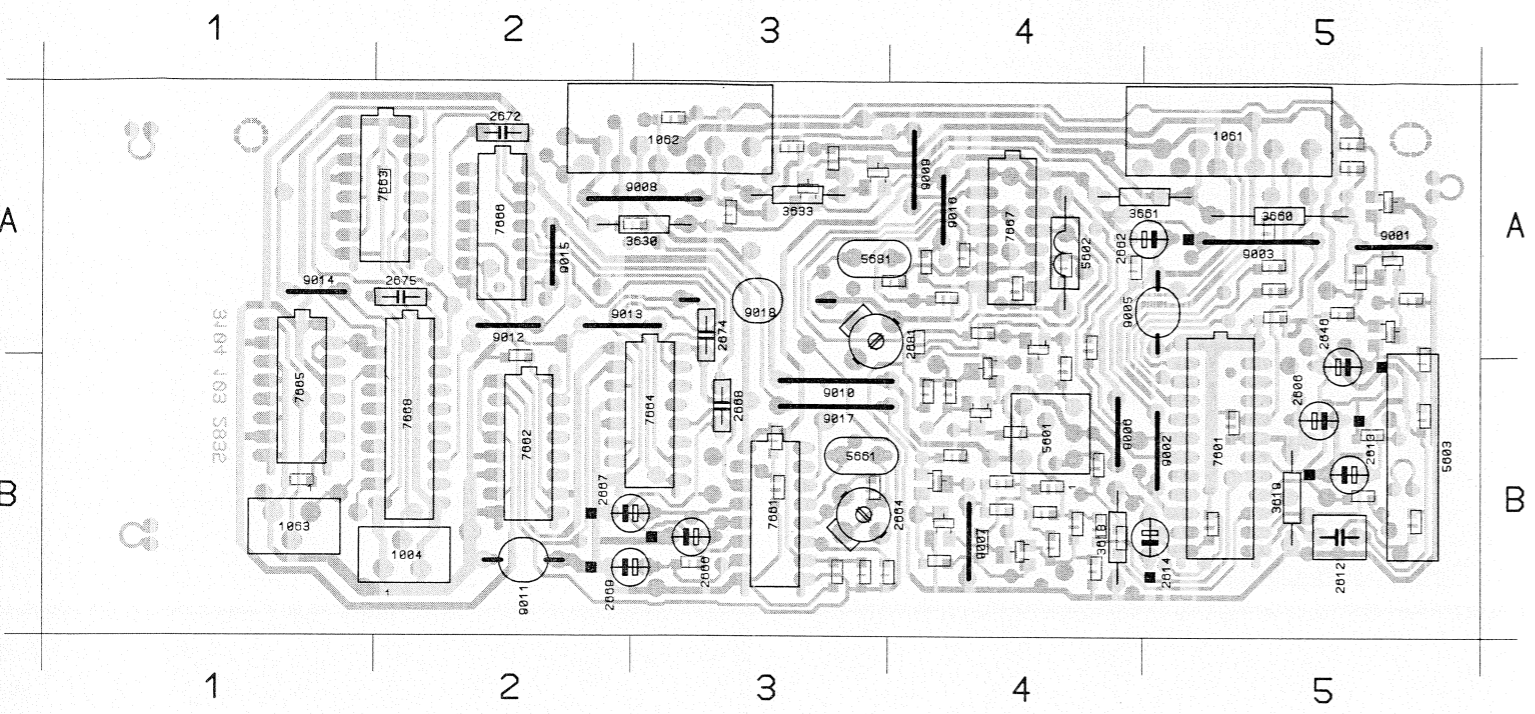


6.5.3 LIST OF ELECTRICAL PARTS APU

Item	Codenumber	Description
2529	4822 124 41738	BIP. 22MU10V
2530	4822 124 41738	BIP. 22MU10V
3406	4822 052 10478	NFR25 4R7
3407	4822 052 10478	NFR25 4R7
3408	4822 052 10478	NFR25 4R7
3411	4822 052 10478	NFR25 4R7
3509	4822 052 10229	NFR25 22R
3510	4822 052 10229	NFR25 22R
3511	4822 052 10229	NFR25 22R
3512	4822 052 10229	NFR25 22R
3513	4822 052 10229	NFR25 22R
3514	4822 052 10229	NFR25 22R
3523	4822 052 10229	NFR25 22R
6505	4822 130 34174	BZX55-C4V7
7400	4822 209 61708	SAA7321GP
7501	4822 209 83163	LM833N
7502	4822 209 83163	LM833N
7503	4822 209 83163	LM833N
7504	4822 209 83163	LM833N
7505	4822 209 71584	74HCT4053P
7506	4822 209 63496	AD7528JN
7507	4822 209 63496	AD7528JN
7508	5322 209 11268	74HCT164P
7510	4822 130 42675	BC818
7511	4822 130 42675	BC818
7512	4822 130 42675	BC818
7512	4822 130 42675	BC818

6.6.1 VIDEO ENCODER PCB, COMPONENT SIDE VIEW

1004 B 2	2006 B 5	2015 B 5	2062 A 4	2070 A 4	2082 A 4	3018 B 4	3030 A 3	3038 B 4	3050 A 5	3053 A 4	7001 A 5	7040 B 4	7005 A 1	9000 B 4	9014 A 1
1001 A 5	2007 B 4	2041 B 4	2063 B 3	2071 A 2	2083 A 4	3019 B 5	3031 B 5	3039 B 4	3051 A 5	3054 A 4	7002 A 4	7041 B 4	7006 A 2	9007 B 4	9015 A 2
1002 A 3	2009 A 5	2042 B 4	2064 B 3	2072 A 2	2082 B 5	3024 A 3	3032 A 3	3040 B 4	3052 B 3	3700 A 5	7004 B 4	7042 A 3	7007 A 4	9008 A 2	9016 A 4
1003 B 1	2010 A 5	2043 B 4	2065 B 3	2073 B 2	2083 B 5	3025 B 5	3033 A 3	3041 A 4	3053 B 3	5001 B 4	7005 A 4	7043 A 3	7008 A 2	9009 A 4	9017 B 4
2002 A 4	2011 A 5	2044 B 4	2066 B 3	2074 A 3	2084 B 4	3026 A 3	3034 A 3	3042 B 4	3054 B 4	5002 A 4	7007 B 4	7044 A 3	7009 A 5	9010 B 4	9018 A 3
2003 B 5	2012 B 5	2045 A 5	2067 B 3	2075 A 2	2085 B 4	3027 A 5	3035 A 5	3043 A 4	3055 B 3	5003 B 5	7008 A 5	7045 B 2	7010 B 5	9011 B 2	
2004 B 4	2013 B 5	2046 B 5	2068 B 3	2076 B 1	2086 A 3	3028 A 3	3036 A 3	3044 B 4	3056 A 4	5004 A 5	7009 A 5	7046 A 1	7011 A 5	9012 A 2	
2005 B 4	2014 B 5	2061 B 3	2069 B 3	2081 A 3	3008 B 5	3029 B 4	3037 B 4	3045 B 4	3058 A 4	5005 A 4	7010 B 4	7047 A 2	7012 A 5	9013 A 3	

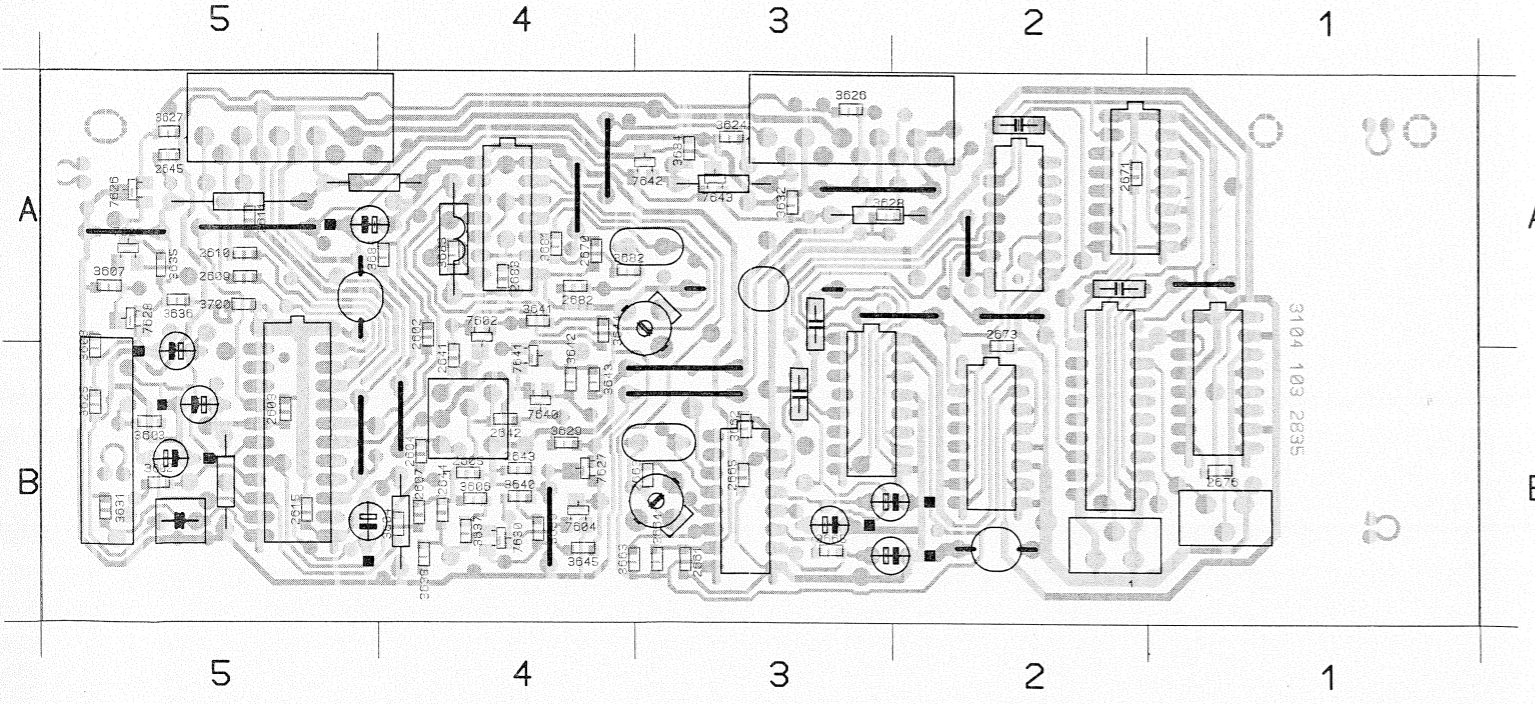


6.6.2 LIST OF ELECTRICAL PARTS VIDEO ENCODER

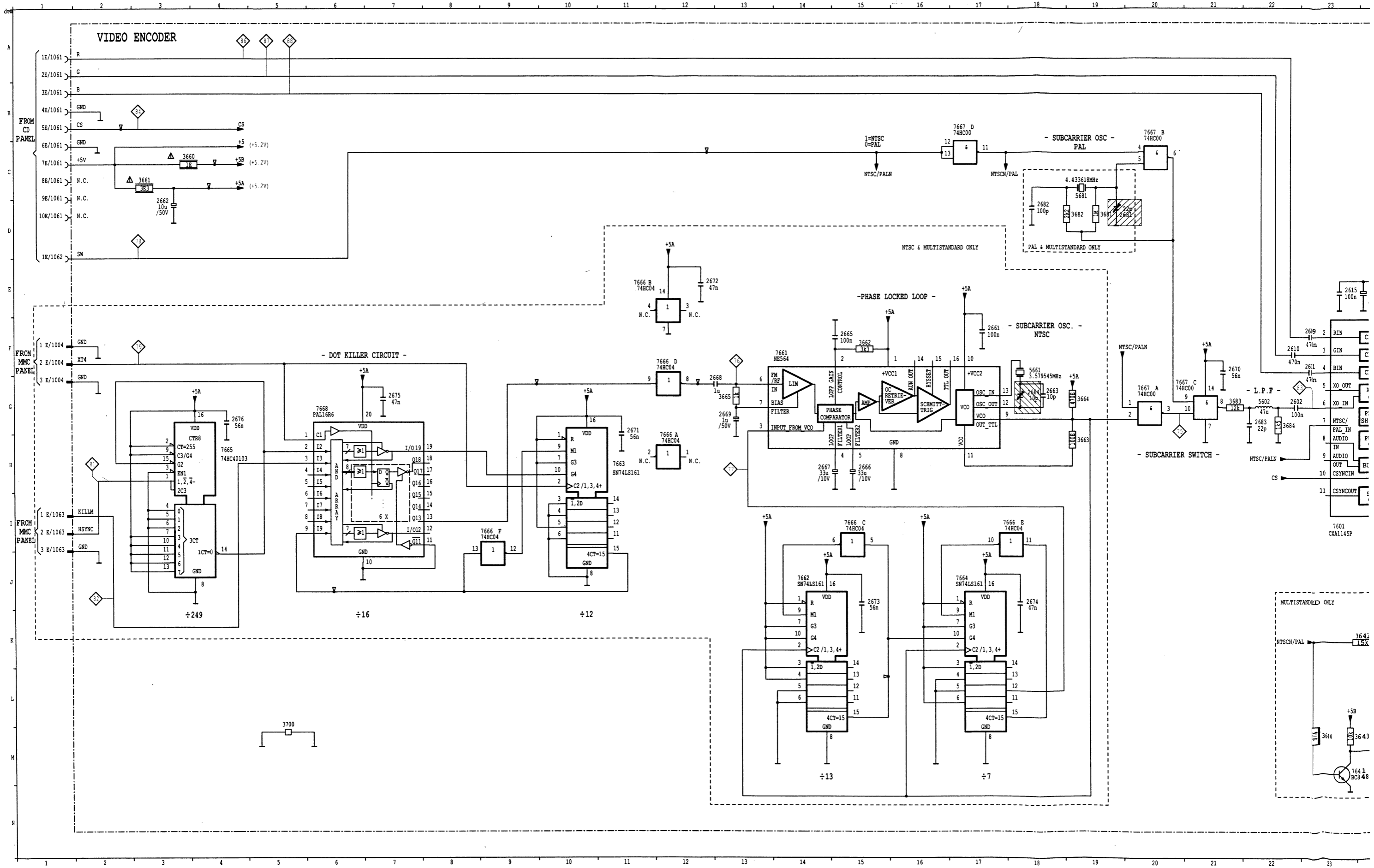
Item	Codenummer	Description
2681	4822 125 50045	TRIM 1P8-22P
3618	4822 052 10228	NFR25 2R2
3619	4822 052 10228	NFR25 2R2
3660	4822 052 10108	NFR25 1R0
3661	4822 052 10108	NFR25 1R0
5681	4822 242 70933	X-TAL 4MHZ433
7601	4822 209 63497	CXA1145P
7604	5322 130 41983	BC858BT
7626	4822 130 61207	BC848
7627	4822 130 61207	BC848
7628	4822 130 61207	BC848
7629	5322 130 41983	BC858BT
7630	4822 130 61207	BC848
7642	4822 130 61207	BC848
7643	4822 130 61207	BC848
7667	5322 209 83218	PC74HC00P

6.6.1 VIDEO ENCODER PCB, COPPER TRACK/SMD SIDE VIEW

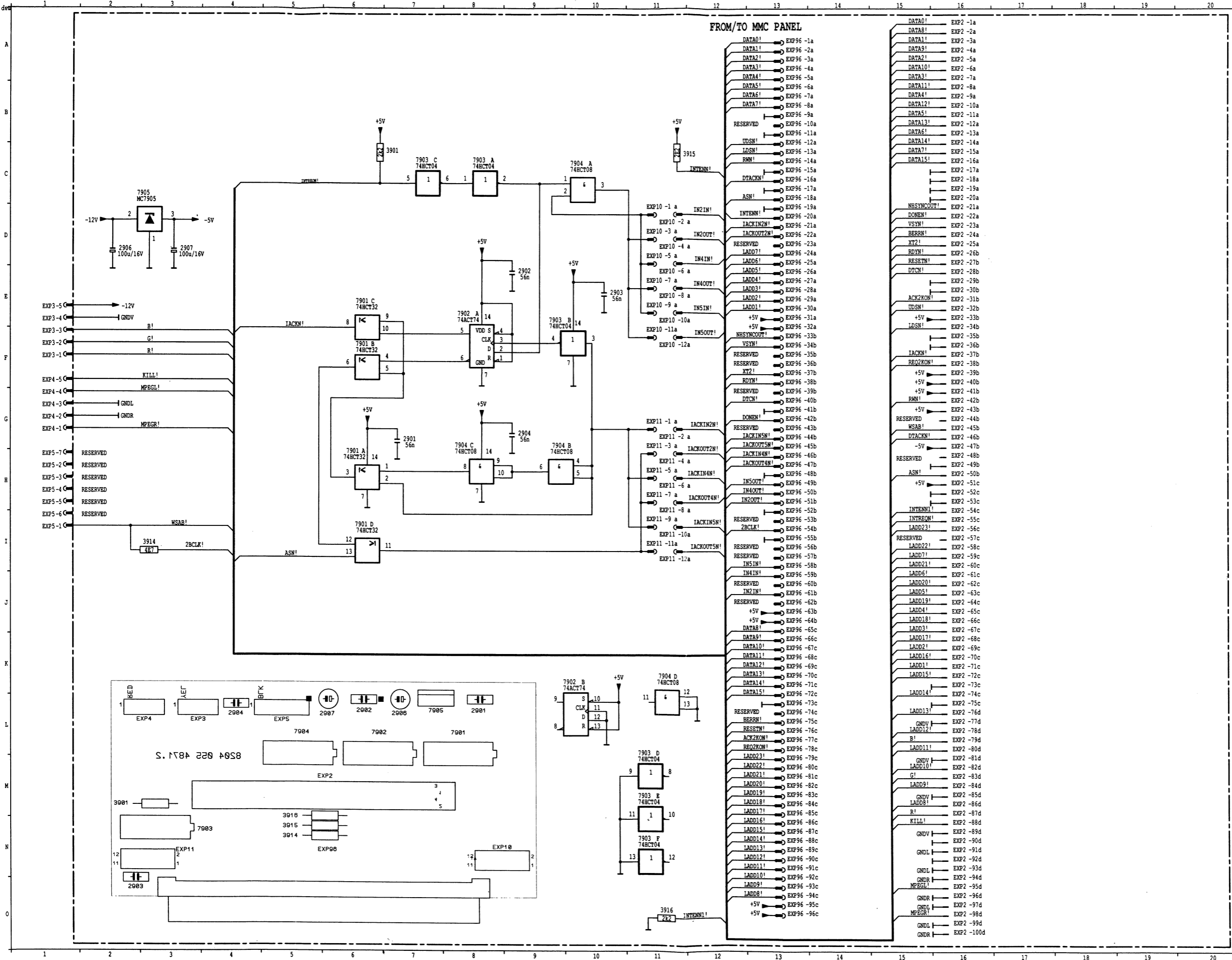
9014 A 1	9006 B 4	7005 A 1	7040 B 4	7001 A 5	3053 A 4	3050 A 5	3038 B 4	3030 A 3	3018 B 4	2082 A 4	2070 A 4	2062 A 4	2015 B 5	2006 B 5	1004 B 2
9015 A 2	9007 B 4	7006 A 2	7041 B 4	7002 A 4	3054 A 4	3051 A 5	3039 B 4	3031 B 5	3019 B 5	2083 A 4	2071 A 2	2063 B 3	2041 B 4	2007 B 4	1001 A 5
9016 A 4	9008 A 2	7007 A 4	7042 A 3	7004 B 4	3700 A 5	3052 B 3	3040 B 4	3032 A 3	3024 A 3	3052 B 5	2072 A 2	2064 B 3	2042 B 4	2009 A 5	1002 A 3
9017 B 4	9009 A 4	7008 A 2	7043 A 3	7026 A 5	5001 B 4	3053 B 5	3041 A 4	3033 A 3	3025 B 5	2073 B 2	2065 B 3	2043 B 4	2010 A 5	1003 B 1	
9018 A 3	9010 B 4	9001 A 5	7001 B 3	7027 B 4	5002 A 4	3054 B 3	3042 B 4	3034 A 3	3026 A 3	3004 B 4	2074 A 3	2066 B 3	2044 B 4	2011 A 5	2002 A 4
	9011 B 2	9002 B 5	7002 B 2	7028 A 5	5003 B 5	3055 B 3	3043 B 4	3035 A 5	3027 A 5	3005 B 4	2075 A 2	2067 B 3	2045 A 5	2012 B 5	2003 B 5
	9012 A 2	9003 A 5	7003 A 1	7029 A 5	5004 A 5	3056 B 3	3044 A 4	3036 A 5	3028 A 3	3007 A 5	2076 B 1	2068 B 3	2046 B 5	2013 B 5	2004 B 4
	9013 A 3	9005 A 5	7004 A 2	7030 B 4	5005 A 4	3058 A 4	3045 B 4	3037 B 4	3029 B 4	3008 B 5	2081 A 3	2069 B 3	2047 B 3	2014 B 5	2005 B 4



6.6.3 VIDEO ENCODER CIRCUIT DIAGRAM



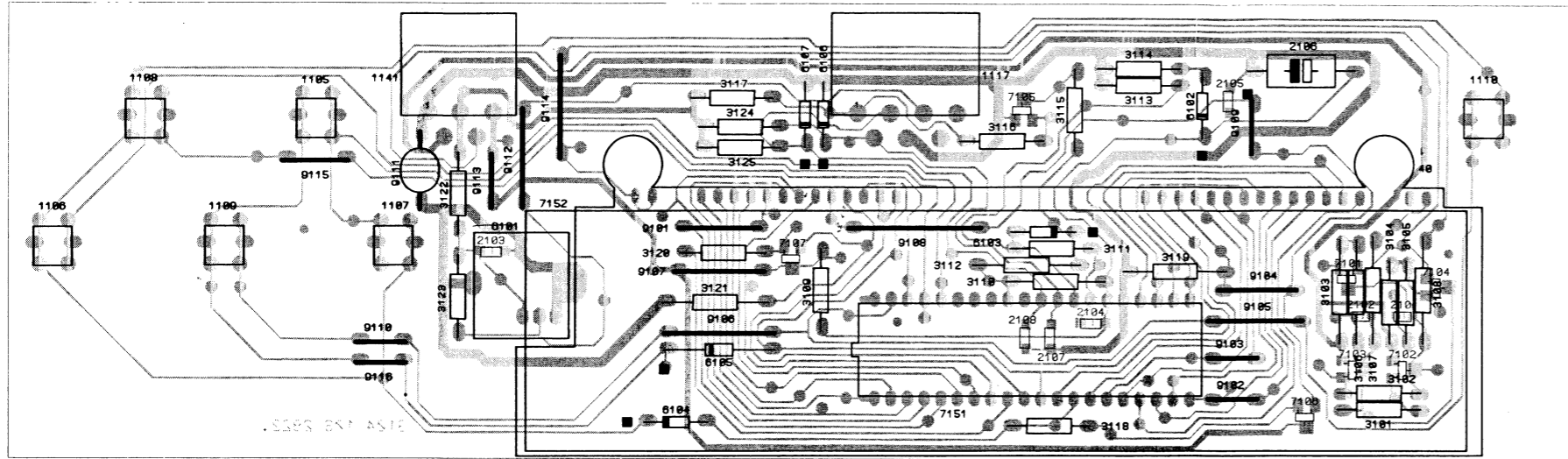
6.7.2 F.M.V. INTERFACE CIRCUIT DIAGRAM



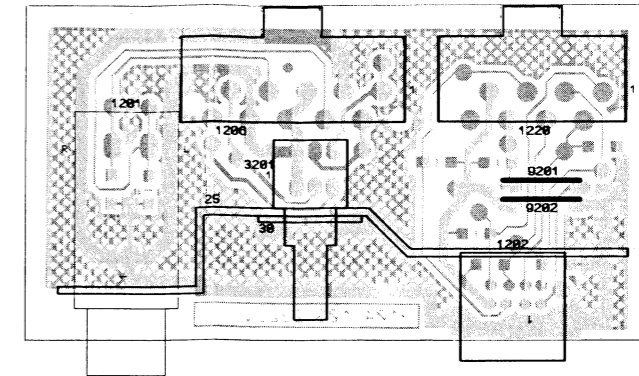
2901	G	7
2902	F	6
2903	E	5
2904	D	4
2905	C	3
2906	B	2
2907	A	1
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2998		
2999		
3000		

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602
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3313 5
2325 2343 5
5303
M24
1
M53
7105
7103
7104
7102
7249
7248
8204 055 4754.7
2230
244
23
M1
3

6.8.1 DISPLAY PANEL PCB. COPPER TRACK/SMD
SIDE VIEW



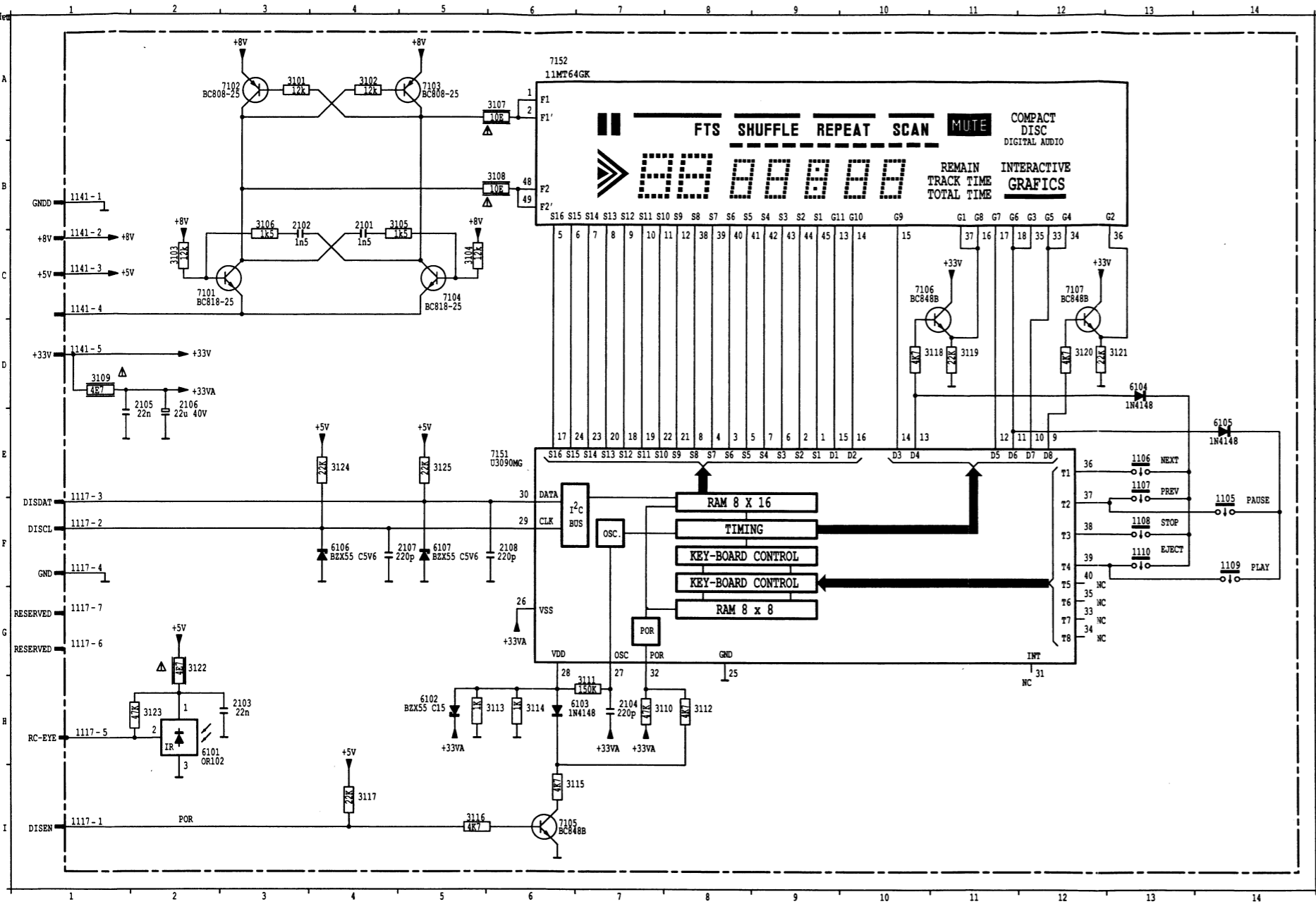
6.8.3 HEADPHONE PANEL



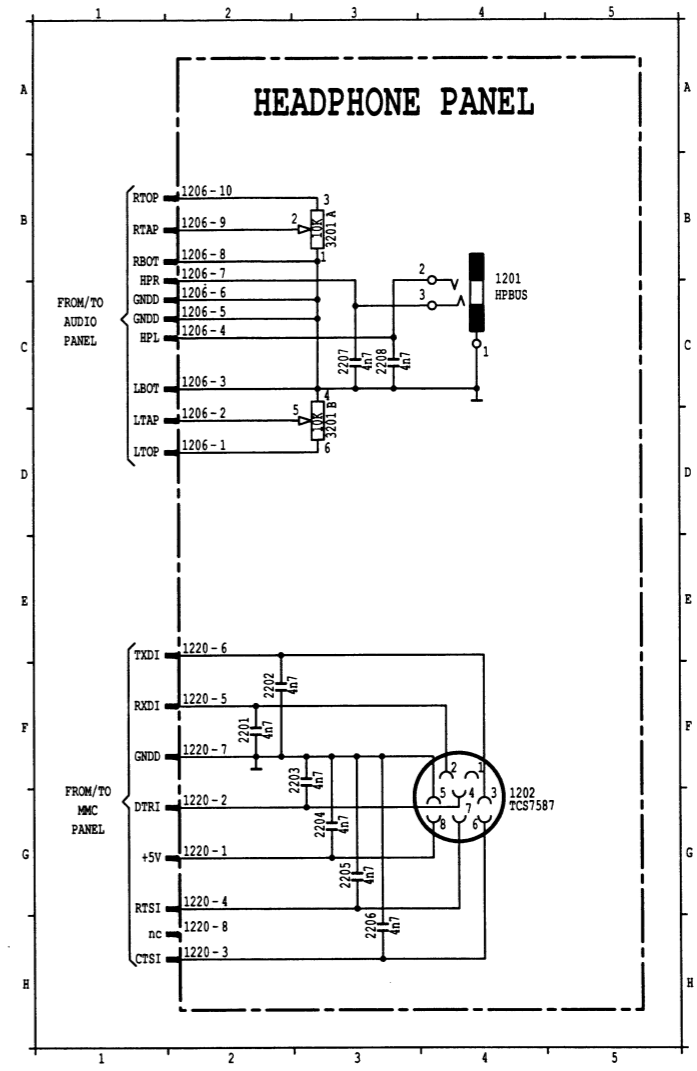
6.8.2 LIST OF ELECTRICAL PARTS DISPLAY PANEL AND
HEADPHONE PANEL

Item	Codenumber	Description
1105	4822 276 13114	TACT SW 4,3MM
1106	4822 276 13114	TACT SW 4,3MM
1107	4822 276 13114	TACT SW 4,3MM
1108	4822 276 13114	TACT SW 4,3MM
1109	4822 276 13114	TACT SW 4,3MM
1110	4822 276 13114	TACT SW 4,3MM
1201	4822 267 30743	HEADPHONE SOCKET
BU-11	4822 267 31289	PORT 1 SOCKET (MOUSE INPUT)
3201	4822 102 10398	VOLUME HEADPHONE POTM.(DUAL 10K LOG)
6101	4822 214 51795	IR-RECEIVER GP1U500X
6102	4822 130 34281	BZX55-C15
6103	4822 130 30621	1N4148
6104	4822 130 30621	1N4148
6105	4822 130 30621	1N4148
6106	4822 130 34173	BZX55-C5V6
6107	4822 130 34173	BZX55-C5V6
7101	4822 130 42696	BC818-25
7102	4822 130 42696	BC818-25
7103	5322 130 42048	BC808-25
7104	4822 130 42696	BC818-25
7105	5322 130 41982	BC848BT
7106	5322 130 41982	BC848BT
7107	5322 130 41982	BC848BT
7151	4822 209 72226	IC U3090MG-40P
7152	4822 130 91068	FL.DISPL. 11-MT-64GK

6.8.4 DISPLAY PANEL AND HEADPHONE PANEL CIRCUIT DIAGRAM

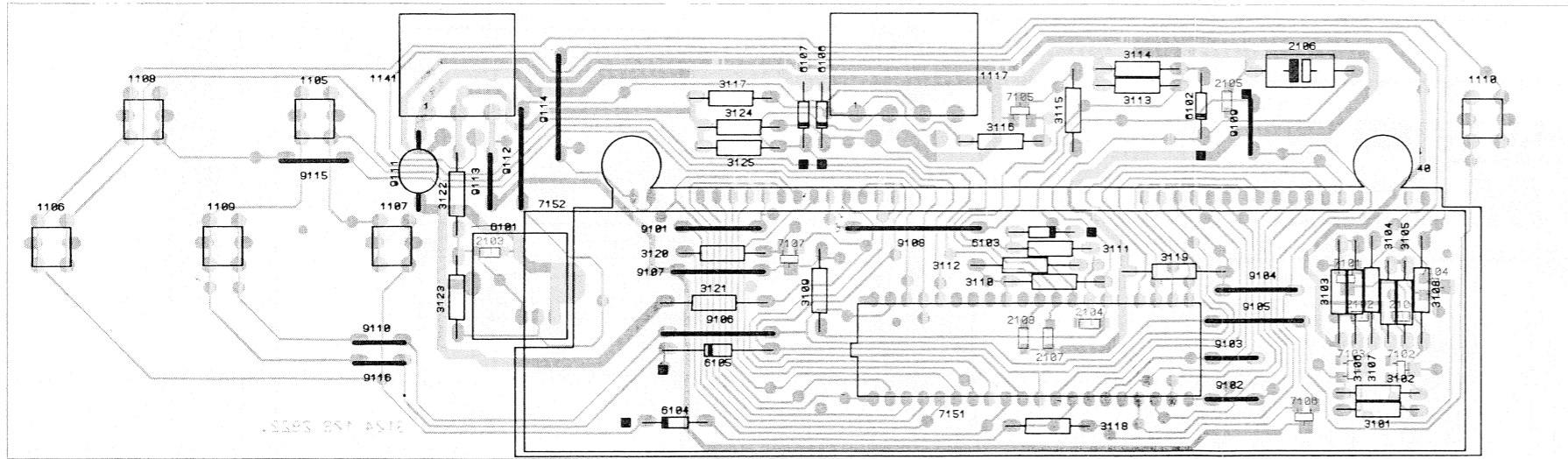


1105 F14
1106 E13
1107 E13
1108 F13
1109 F13
1110 F13
1111 F13
1112 F13
1113 F13
1114 F13
1115 F13
1116 F13
1117 F13
1118 F13
1119 F13
1120 F13
1121 F13
1122 F13
1123 F13
1124 F13
1125 F13
1126 F13
1127 F13
1128 F13
1129 F13
1130 F13
1131 F13
1132 F13
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1142 F13
1143 F13
1144 F13
1145 F13
1146 F13
1147 F13
1148 F13
1149 F13
1150 F13
1151 E A 6
1152 E A 6
1153 E A 6
1154 E A 6
1155 E A 6
1156 E A 6
1157 E A 6
1158 E A 6
1159 E A 6
1160 E A 6
1161 E A 6
1162 E A 6
1163 E A 6
1164 E A 6
1165 E A 6
1166 E A 6
1167 E A 6
1168 E A 6
1169 E A 6
1170 E A 6
1171 E A 6
1172 E A 6
1173 E A 6
1174 E A 6
1175 E A 6
1176 E A 6
1177 E A 6
1178 E A 6
1179 E A 6
1180 E A 6
1181 E A 6
1182 E A 6
1183 E A 6
1184 E A 6
1185 E A 6
1186 E A 6
1187 E A 6
1188 E A 6
1189 E A 6
1190 E A 6
1191 E A 6
1192 E A 6
1193 E A 6
1194 E A 6
1195 E A 6
1196 E A 6
1197 E A 6
1198 E A 6
1199 E A 6
1200 E A 6

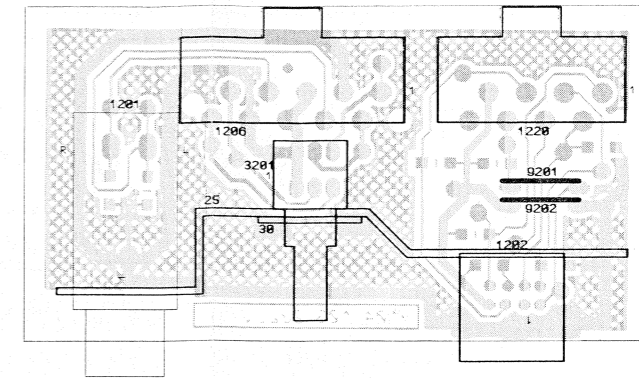


1201 C 4
1202 C 4
1203 C 4
1204 C 4
1205 C 4
1206 C 4
1207 C 4
1208 C 4
1209 C 4
1210 C 4
1211 C 4
1212 C 4
1213 C 4
1214 C 4
1215 C 4
1216 C 4
1217 C 4
1218 C 4
1219 C 4
1220 C 4
1221 C 4
1222 C 4
1223 C 4
1224 C 4
1225 C 4
1226 C 4
1227 C 4
1228 C 4
1229 C 4
1230 C 4
1231 C 4
1232 C 4
1233 C 4
1234 C 4
1235 C 4
1236 C 4
1237 C 4
1238 C 4
1239 C 4
1240 C 4
1241 C 4
1242 C 4
1243 C 4
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1269 C 4
1270 C 4
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1272 C 4
1273 C 4
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1283 C 4
1284 C 4
1285 C 4
1286 C 4
1287 C 4
1288 C 4
1289 C 4
1290 C 4
1291 C 4
1292 C 4
1293 C 4
1294 C 4
1295 C 4
1296 C 4
1297 C 4
1298 C 4
1299 C 4
1300 C 4

6.8.1 DISPLAY PANEL PCB. COPPER TRACK/SMD
SIDE VIEW



6.8.3 HEADPHONE PANEL



6.8.2 LIST OF ELECTRICAL PARTS DISPLAY PANEL AND
HEADPHONE PANEL

Item	Codenumber	Description
1105	4822 276 13114	TACT SW 4,3MM
1106	4822 276 13114	TACT SW 4,3MM
1107	4822 276 13114	TACT SW 4,3MM
1108	4822 276 13114	TACT SW 4,3MM
1109	4822 276 13114	TACT SW 4,3MM
1110	4822 276 13114	TACT SW 4,3MM
1201	4822 267 30743	HEADPHONE SOCKET
BU-11	4822 267 31289	PORT 1 SOCKET (MOUSE INPUT)
3201	4822 102 10398	VOLUME HEADPHONE POTM.(DUAL 10K LOG)
6101	4822 214 51795	IR-RECEIVER GP1U500X
6102	4822 130 34281	BZX55-C15
6103	4822 130 30621	1N4148
6104	4822 130 30621	1N4148
6105	4822 130 30621	1N4148
6106	4822 130 34173	BZX55-C5V6
6107	4822 130 34173	BZX55-C5V6
7101	4822 130 42696	BC818-25
7102	4822 130 42696	BC818-25
7103	5322 130 42048	BC808-25
7104	4822 130 42696	BC818-25
7105	5322 130 41982	BC848BT
7106	5322 130 41982	BC848BT
7107	5322 130 41982	BC848BT
7151	4822 209 72226	IC U3090MG-40P
7152	4822 130 91068	FL.DISPL. 11-MT-64GK

7 DIAGNOSTICS

7.1 TROUBLESHOOTING AND REPAIR

This section contains some guides to aid the technician in troubleshooting the CDI player. The CD servo section and Audio Processing Unit are similar to any CD player. Thus, the same techniques for troubleshooting a CD player may be used. Added features in servicing the CDI player is the Low Level Test and the Service Shell, see section 5. "Service Software". The Low Level Test needs a VT100 terminal or a Service PCB as an extra tool to run and test the functioning of the MMC. The Service Shell provides tests for the Video, CD Servo, and Audio circuits. Section 5.2 covers all the Service Shell test procedures.

All circuit board assemblies can be serviced to the component level except the MMC board. Due to the complexity of the MMC board, replacement is recommended when defective. The CDM-9 CD Mechanism is also replaced as an assembly. Disassembly instructions and exploded views are provided in the service manual see section 4.1.7.2.

Troubleshooting hints:

Symptom: Service Shell cannot be started with the test plug.

Possible fault: Connections between port 1 and Slave Microprocessor may be bad. Test plug could be wrong. Slave Microprocessor may be defective.

Hint: If the Player Shell cannot be started, perform the Low Level Test (LL TEST).

7.1.1 Troubleshooting the Power Supply

The Power Supply can be checked and serviced after removal from the main chassis. The connectors to the player's circuits (the loads) may be unplugged to check the power supply. However, the 5Vdc source must be loaded with a 5 ohm resistor (10 watts), to provide a current of about 1 amp. (Note: if a load is not used, the Overvoltage Protect circuit is activated.) A variac may be used to slowly increase the ac voltage, while checking the 5Vdc source. As the ac is increased, an audible squeal is heard between 10 and 50 volts ac (starting of the power supply).

Service hints:

- * If the fuse is open, Switching Transistor 7002 is probably shorted. Also check transistors 7001 and 7004.
- * There are two possible error conditions if the power supply squeals:
 - 1) there may be a short circuit in the secondary side of the power supply circuit or in the other player circuits.
 - 2) the overvoltage protection circuit is activated. If the overvoltage protection is energized, 7007 becomes hot. Check the control circuit.

7.1.2 Troubleshooting and Service the MMC panel

The MMC board is replaced as a module when defective. The technician must know the functions of the MMC Unit to diagnose a CDI player. The CDI player contains some built-in diagnostics to aid in troubleshooting. One diagnostic tool is the Service Shell (see section 5.2) and the other is the Low Level Test or LL Test (see section 5.1). The LL Test should be performed if there is access to neither the Player Shell nor the Service Shell. If the Low Level MMC test indicates a fault, replace the MMC Unit. If the Low Level Test Cannot be initiated, check the power sources and main clock signals on the MMC board (see section 7.2.5). If all supplies and clock signals are present, replace the MMC Unit.

7.1.3 CD-part and Audio Section Troubleshooting

A problem in the CD-I player can be isolated to a particular circuit by carefully observing the symptoms. For example, if there is no audio, but a picture from a CD-I disc is displayed, it is obvious that the CD Servo and decoding circuits are functional. Therefore the fault can be isolated to the audio decoding circuits only. Or the symptom may be opposite, the audio circuits may be working, but not the video. Again, the servo circuits must be functioning. Troubleshooting of the video decoding should then be followed.

When there is a symptom indicating a fault in the CD Drive circuitry, troubleshooting techniques used in CD players can be followed since the CD Unit portion of the CD-I player is basically a CD player (refer to the CD Unit schematic diagrams in the service manual). If the CDM does not start, check for Vdd, clock, and reset on the CD Drive Microprocessor. If these signals are present, perform the X-bus test in the Service Shell. Also check for activity on the X-bus and SPI-bus. If there is a communication failure, proceed with the MMC Low Level Test to determine if there is a failure in the system control circuitry. If the communication buses are functional, check the CD servo circuits using the Service Shell test modes. These modes are the standard CD servo test modes to test the OPU, turntable and swing arm. If there is a failure in the servo test modes, further checks with measurements on the CD panel (see section 7.2.2) should reveal the fault.

If the servo circuits are functioning, check the decoder circuits. Activity should be seen on the I²S (DAAB, CLAB, and WSAB) and subcode (SCAB and SDAB) lines from the SAA7310 Decoder IC. If there is no activity, check the supply (Vdd) and input signals (HF, XIN). If there is activity, check the ADOC circuitry.

When the servo and decoder circuits are functioning properly, there may be a problem in the Audio Processing Unit. The APU Panel plugs in to the CD Unit circuit board (see APU schematic and Wiring Diagram in the service manual). Interconnections are thus made to the CD Unit via two connectors on the bottom of the board. The three connectors at the top of the APU provide interconnection with the MMC Panel. Extension connectors (part number 4822 321 22268; requires 2 for service) are available to gain access to the bottom connectors for troubleshooting. Supply voltages and signals going into the APU Panel can be checked at the connectors. For example, the I²S bus from the MMC panel can be checked on connector A16 (7 Pin connector) on the top of the board. Also, the analog output can be checked at connector A9 on the bottom of the board. If the input signals are present, but not the analog audio at the output, then a problem exists on the APU. Further checks of the APU circuitry should be followed. If the analog audio signals are present at the output of the APU, then the signal route on the CD Unit should be followed to find the fault. The Kill and buffer circuitry on the CD Unit should be checked for proper operation.

7.1.4 Video Section Troubleshooting

Note 1: refer to the Video Encoder Circuit Diagram, MMC Circuit Diagram, and the Interconnect Wiring Diagram in the service manual.

Note 2: Use two service extension cables (part number 4822 321 22267) to allow easy access to the Video Encoder Panel.

The symptoms displayed can help the technician isolate the problem to a particular circuit. The following examples illustrate how a fault can be isolated.

Symptom 1: the player shell is displayed, but video from the disc cannot be displayed. If this condition exists, the Video Encoder Panel and video analog circuits are functioning. Since the player shell is displayed, the video synthesizer circuit is functioning. However, there must be a fault on the MMC Panel, since this is where the video decoding takes place. Thus the problem is isolated to the video decoding section on the MMC Panel.

Symptom 2: no video. This symptom may be caused by either the Video Encoder Panel or by the MMC Panel. A few voltage and signal measurements can quickly isolate the problem. Hint, also check all the video outputs: S-video, RF, and CVBS. If video is not present from any output, check the RGB, composite sync, and power source inputs from the CD Unit to the Video Encoder Panel (Connector 1061 on the bottom of the Video Encoder Panel).

If these signals are present, the MMC Panel's decoder circuits are functional. Further checks of the Video Encoder circuit can isolate the problem further. Check the Video Encoder IC. Also check Vcc1 and Vcc2 to the Video Encoder IC. If both sources are missing, check Resistor 3660. If Vcc1 is missing, check Resistor 3618 and if Vcc2 is missing, check 3619.

Symptom 3: no color. This symptom is most likely caused by a problem in the ENCODER circuit. Check the subcarrier oscillator at Pin 6 of the Video Encoder IC. If this signal is present (correct frequency), check the chroma output signal at Pin 15. If there is no chroma output, IC7601 may be the fault. Also check for short circuits between pins of the IC. If the chroma is present, check the chroma input at Pin 17. If the chroma is not present here, check the coupling components between Pins 15 and 17. If there is chroma at this point, check the composite output at Pin 20. If the chroma is missing, suspect the Video Encoder IC (IC7601).

7.2.1 Measurements & adjustments power supply 1006

CAUTION.

Never turn on the power supply if no load resistor has been connected.

- For service purposes you only have to connect a load resistance to the + 5,2V supply voltage. Use a 4 Ohm / 25W resistor. Of course in that case the other supply voltages are not in accordance with the specification.
- Safety regulations require that the set under repair should be restored to its original state and that components identical to the ones specified should be used.
- For reasons of safety, components marked should be replaced by identical components. For code numbers refer to the parts list of electrical components.

Beware of the live parts!

7.2.1.1 Checkpoints

Check the following supply voltages:

SUPPLY	NOMINAL VALUE (DC)	CONNECTOR/PINS
+ 5,2V	+ 5,3V DC	P0006 pin 4
+ 12 V	+ 12,1V DC	P0005 pin 1 or M7 pin 8 (MMC Panel)
- 12 V	- 12,1V DC	P0005 pin 2 or M7 pin 7 (MMC Panel)
- 8 V	- 8V DC	P0004 pin 6 or C1 pin 3 (CD Panel)
+ 8 V	+ 8V DC	P0004 pin 7 or C1 pin 2 (CD panel)
+ 30 V	+ 28,5V DC	P0004 pin 8 or C1 pin 1 (CD panel)

All voltages have been measured relative to earth.

7.2.1.2 Adjustments

Adjustment + 5,2V supply voltage

Adjust R3020 for a voltage of 5.3V DC \pm 40 mV on test point 51.

For practical reasons it is also possible to measure at pin 3 of connector G12 on the extension board.

7.2.2 Measurements & adjustments CD panel 1004

In the circuit diagrams and on the drawings of the panels measuring points are marked with: .

Some times signals to be measured are pointed as for example: IC7181 pin1.

All DC signals are measured with an universal electronic voltmeter.

All AC signals are measured with an oscilloscope

7.2.2.1 Lasercurrent.

The lasercurrent is adjusted in the CDM9 and is a factory adjustment. After replacing a defective CDM the laser current does not need to be adjusted.

Play track 1 of testdisc 5, the voltage across item 3114(measuring point 1 and point 2) on the CD panel should be: 0,7 V / DC \pm 10 %.

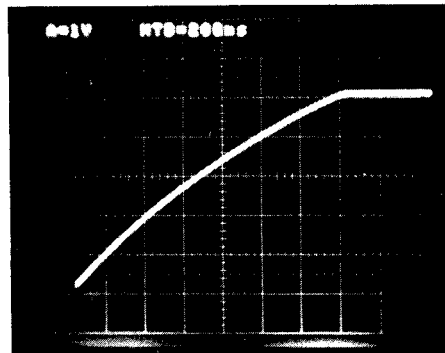
7.2.2.2 Focus signal.

Play track 1 of testdisc 5, the voltage across item 2151 (measuring point 3 and GND) on the CD panel should be: + 400 mV / DC \pm 10%.

7.2.2.3 Starting signal.

Insert a disc and measure across item 2112 (measuring point 4 and GND).

After pushing the play button the next picture appears on the oscilloscope:

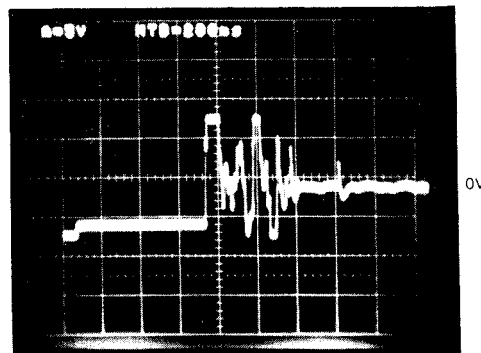


The signal is triggered by the Si/RD signal on IC7101 pin 6.

7.2.2.4 Motorcontrol signals.

Insert testdisc 5.

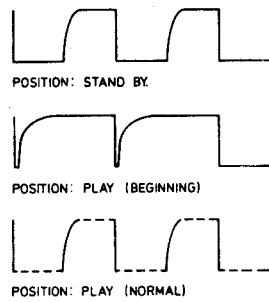
Measure across IC7181 pin1 and GND, after pushing the play button the next picture should appear on the oscilloscope.



After a while, when playing track 1, the voltage should be: - 1.7 V DC \pm 10%

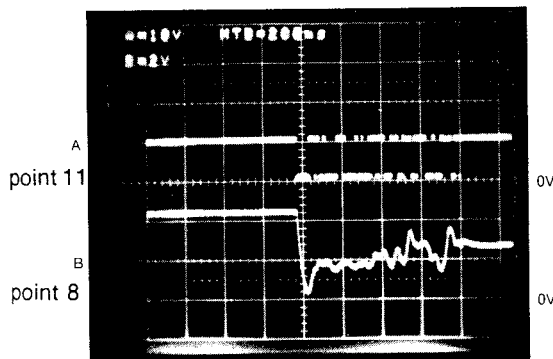
Play track 1 of testdisc 5, the voltage across measuring point 6 and ground should be: 3.2 Volt DC \pm 10%

Signal across measuring point 7 and GND should be :



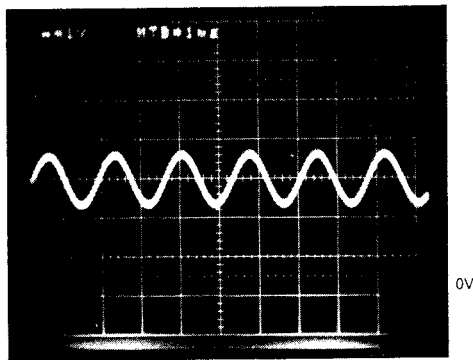
38 849 A12

Insert test disc 5. Across measuring point 8 and GDN the next picture should appear on the oscilloscope after pushing the play button



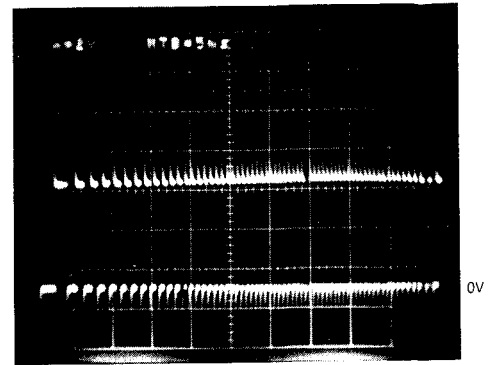
7.2.2.5 Radial error circuit signals.

- Voltage across measuring point 18 and GND: 2,6 V / DC $\pm 10\%$.
- Voltage across measuring point 19 and GND: 110 mV / DC $\pm 10\%$ in PLAY mode.
- Voltage across measuring point 21 and GND: 1,2 V / DC $\pm 10\%$ in PLAY mode.
- Voltage across measuring point 22 and GND:



Voltage across measuring points 23,24,26 and 27 depending on playing mode, 0 V if LOW or 5V if HIGH

For measuring point 28 and 33 put the player in the service shell on CD drive test mode 2. The voltage across point 28 and GND should be:



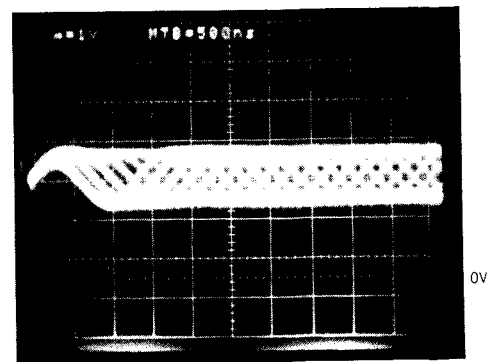
7.2.2.6 Clock signal μP IC7201

Measuring point 29: clock signal $f = 4\text{MHz}$.

7.2.2.7 Decoder signals

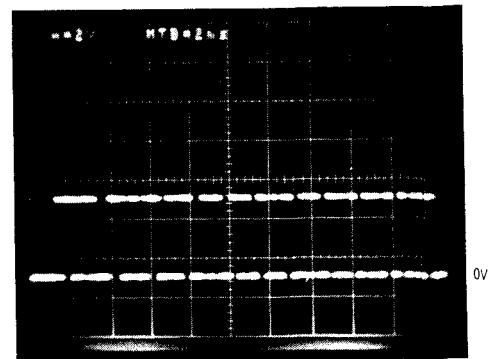
Play track 1 of testdisc 5.

The signal across measuring point 31 and GND should be:



Insert testdisc 5 and put the player in the service shell on CD drive test mode 2.

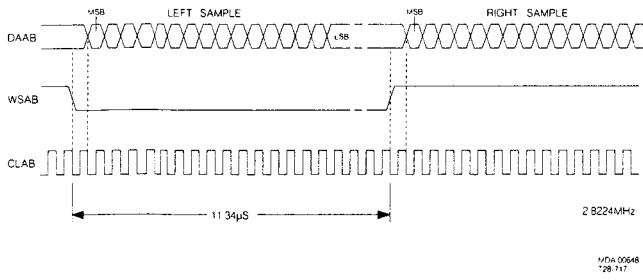
The signal across measuring point 32 should be:



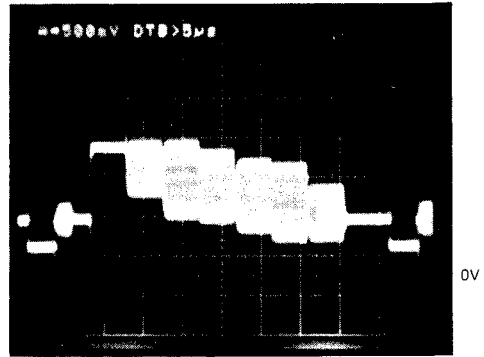
Measuring point 34: clock signal $f = 11.289.600 \text{ Hz}$.
 Voltage across measuring point 37 and 37: 775 mV / DC $\pm 10\%$

Measuring points 38: LOW. If the blackdot track of testdisc 5A is played then pulses activity should be measured on this point.

Measuring point 39,41 and 42:



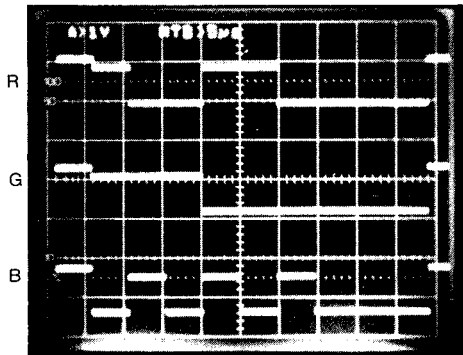
Measuring point 48:



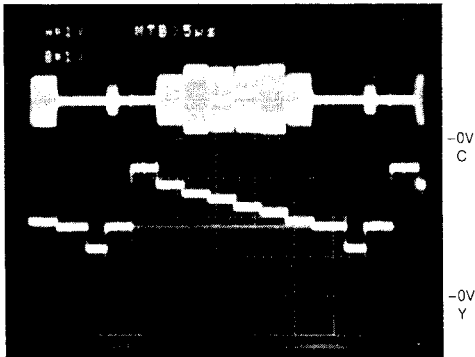
7.2.2.8 Video signals

Put the player in the service shell on testimage (colorbar).

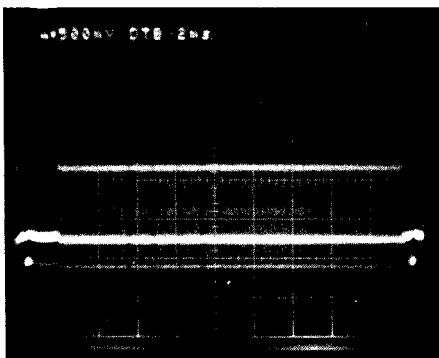
Measuring point 43 and 44:



Measuring point 46:



Measuring point 47:



7.2.3 Measurements & adjustments audio processing unit

Select the submenu "MMC slave" of the Service Shell, see section 5.2. With this menu we can check besides the remote control functions also the audio functions **L-R** and **mono/stereo**. This audio function can only be checked when an audio-disc is inserted. When any disturbances occur, the following checks/measurements can be performed (2 % 8).

Required test discs:

Use an arbitrary Digital Audio disc in the **service shell**, submenu **MMC slave**.
 Testdisc no. 5 - 5A (4822 397 30096 - SBC 426)
 Use launch disc or arbitrary CD-I disc which contains audio levels A-B-C and/or CD-DA
 Audio signals disc (4822 397 30184 - SBC 429)

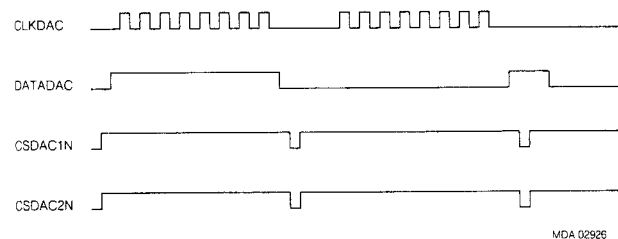
Extension PCB's.

For measurements at this PCB it is necessary to create a service position for the APU panel.
 This is done with the extension PCBs 6 pole service code 4822 321 22268
 The slave processor (7206) on the MMC panel controls the attenuators 7506 and 7507 via te serial/parallel convertor (7508). One step of the counters in the **service shell** menu corresponds with 1dB.

7.2.3.1 Slave processor data

Check whether the signals appear on test/measurements points 66 % 69 (connector A11 pin 1%4) from the slave processor.

- 66 — CLKDAC
- 67 — DATADAC
- 68 — CSDAC1N
- 69 — CSDAC2N



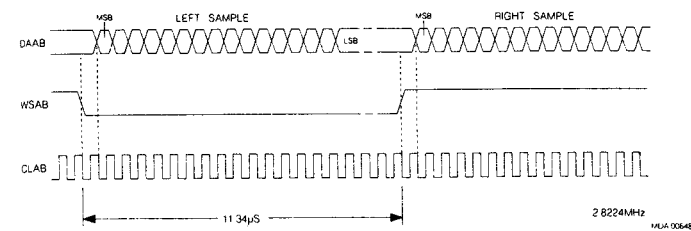
These signals are very hard to recognize on an oscilloscope during the normal application. Only in the **service shell** and controlling the attenuators you can observe activity .
 If there is any activity on one of the lines 66 % 69 one can suppose that the information of this signals are oke. This is also to be considered for the data lines D0 % D7.

If the control signals not appear or deviates, check the connections from MMC panel Plug M11 pin 1 % 4.

If no disturbances, check the data outputs D0 % D7 of IC7508.

7.2.3.2 I2S signals

Check whether the signals, given below, appear on the test points 57 - 58 - 59 (connector A016 pin 2 - 4 - 6)
 Time base related only to CD-DA.



If deviates, check connections from MMC panel, plug M16 pin 2-4-6

7.2.3.3 Xin clock signal

(testpoint 61, connector A023 pin 2)

Play a CD-DA track.
 The frequency of the Xin signal must be:
 11,2896 MHz (CD-DA.)

Play CD-I audio.
 The frequency of the Xin signal must be:
 9,767 MHz for CD-I level A and CD-I level B.
 4,838 MHz for CD-I level C.

If deviates check connection from MMC panel, connector M23 pin 1 % 3 and I²S interface on MMC panel.

7.2.3.4 DEEMP signal

(testpoint 56, connector A016 pin 1)
 Insert test disc 5 or 5 A and during track 14 (recorded without pre-emphasis) the signal DEEMP should be low. (0 V.)
 During track 15 (recorded with pre-emphasis) this signal DEEMP should be high (+ 5V.)

If deviates, check the connection from MMC panel, plug M16 pin 7.

7.2.3.5 FILTERN signal

(testpoint 62, connector A016 pin 7)
 Insert CD-I disc which contains audio levels A-B-C and/or Digital audio.
 This signal FILTERN should be high (+ 5V.) In case a track is played back with audio level C (speech).
 The signal FILTERN should be low (0 V.) in case of level A or B or DA.

7.2.3.6 KILL signal

(testpoint 54, connector A025 pin 6)
 This KILL signal must be +12V during reset.
 In normal/play position this signal is - 8 V.

If deviates check the connection with CD-panel (C025 pin 6).

7.2.3.7 Performance check APU

Position digital audio
 — Insert Audio signals test disc 1, SBC 429
 — Play track no. 1. (1kHz sinus signal L + R 0dB)
 — The level on testpoint 63 and 64 should be:
 0.9 Vrms ± 2dB

If this level deviates check first the signals

FILTERN	62	step 6,
KILL	54	step 7 and
Xin	61	step 4.

— The level on testpoint 71 and 72 should be:
 2 Vrms ± 3dB.

Position audio level c
 — Insert CDI disc
 — Play track with audio level C, 1 KHz L + R, 0 dB.
 — The level on testpoint 63 and 64 should be:
 0.9 Vrms ± 3 dB

If this level deviates check first the signals

FILTERN	62	step 6 and
KILL	54	step 7.

— The level on test point 71 and 72 should be:
 2 Vrms ± 3dB.

7.2.4 Measurement & adjustments video encoder unit 1003

Required test equipment.

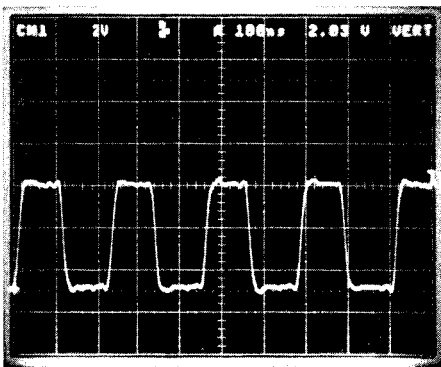
- Electronic voltmeter
- Oscilloscope
- Frequency counter

7.2.4.1 Check of PAL subcarrier .

- Player switched off.
- Connect frequency counter to testpoint 83, (Pin 6 IC 7601) and turn on the player.
- The frequency on testpoint 83 should be; 4 433 618 Hz. \pm 50 Hz.
- The amplitude on testpoint 83 should be in between; 400 mV and 1000 mVpp
- If the frequency of this signal deviates, perform alignment of trimmer 2681.

Adjustment PAL sub carrier oscillator.

- Player switched off.
- Standard switch NTSC/PAL (SK-2) in position 625, PAL .
- Connect frequency counter to testpoint 75 ,Pin 8 IC 7667 and turn on the player.
- Adjust with trimmer 2681, the frequency on testpoint 75 at 4 433 618 Hz. \pm 50 Hz.

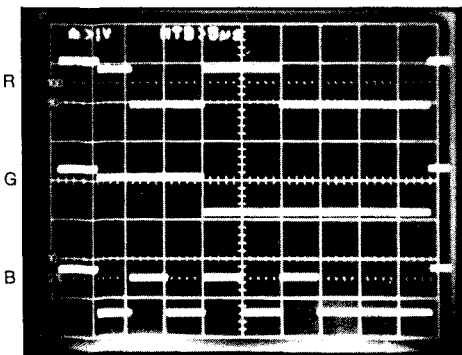


7.2.4.2 Check of standard control signal SW

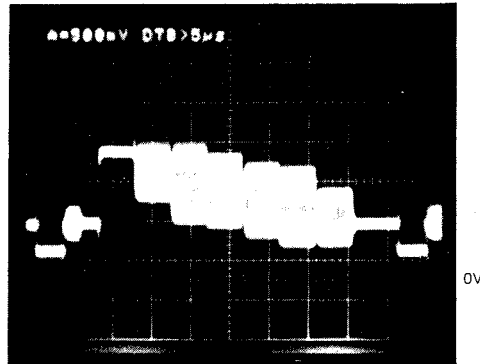
The control signal SW on testpoint 78,(pin 1 of connector E 1062) should be low (0 V).If this signal deviates check the connections to the CD panel print connector E1063 pin 1 and the connection from the CD panel to the MMC panel.

7.2.4.3 Check of RGB input signals

On the given photo below the signals are given for R - G - B.
On Testpoints 86 87 88. (points 1-2-3 of connector E1062)

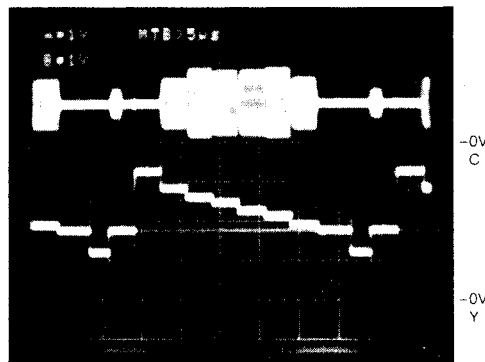


Check of Output signals for CVBS - Y / C.



PAL-CVBS signals Testpoint 89

Video signal	1000 mV _{pp}
White level	710 mV _{pp}
sync	290 mV _{pp}
Burst	290 mV _{pp}



PAL- Y/C Sign. Testpoint 91/92

Video signal	1000 mV _{pp}
White level	710 mV _{pp}
sync	290 mV _{pp}
Chroma	300 mV _{pp}

7.2.5 Measurements and adjustments MMC panel 1001

Required equipment:

Multimeter
Display terminal type Digital VT100 or equivalent
Digital oscilloscope
Analog oscilloscope
Timer/counter

7.2.5.1 Measurements Supply:

Check if the following voltages are present at connector M1.

pin 1M1: +5V +/- 5% (= digital power supply)
pin 2M1: +5V +/- 5% (= digital power supply)
pin 3M1: ground (=digital ground)
pin 4M1: ground
pin 5M1: ground (=analog ground)
pin 6M1: +5V +/- 5% (analog supply)
pin 7M1: -12V +/- 10%
pin 8M1: +12V +/- 10%

7.2.5.2 Clock signals:

Carry out measurements just after hardware reset.
This is done each time after pressing the OPEN/CLOSE button or after power-on.

System clock = 30.0000 MHz +/- 1500 Hz (PAL)
This system clock must be present at the following points:
IC7201 pin 30
IC7101 pin 119
IC7110 pin 119

At IC 7201 pin 29 Clock divided by two must be present:
15.000 MHz (=30.000 : 2).

At IC7201 pin 69 the UART clock of 68070 must be present:
Frequency 4.9152 MHz ± 250 Hz

At IC7241 pin 32 the DUART clock must be present.
Frequency 3.68684 MHz ± 90 Hz

At IC7206 pin 39 clock of '68HC05' must be present.
Frequency 4.000 MHz ± 100 Hz

At IC7301 pin 94 the clock of the CDIC must be present:
Frequency 22.5792 MHz ± 1100 Hz.

At IC7306 pin 16 the DSP clock must be present.
Frequency 7.5264MHz ± 380 Hz

At pin 2M24 the '2B-clock' must be present.
Frequency 11.2896 MHz ± 560 Hz

Carry out measurements at pin 2M4. Clock of 'XT4' must be present.
Frequency 7.5000 ± 380 Hz
The frequency at pin 8M3 'COXN' must be 75kHz +/- 25kHz. (saw thooth signal). Short circuit capacitor 2228 and carry out measurements at IC7318 pin 9.
Frequency 19.3536 ± 100 KHz.

7.2.5.3 I2S interface:

Check connector M16
1M16: FILTERN : 0V
2M16: DAAB
4M16: CLAB : frequency 2.8224 MHz (only for CD-DA)
6M16: WSAB : frequency 44.1 KHz (only for CD-DA)
7M16: DEEM : 0V (only for CD-DA and only if deem-phasis track is played)

7.2.5.4 Reset circuitry:

Press the OPEN/CLOSE button at front panel and measure the 'RESETCD' time (low!). This 'low' time must be 140ms ± 20 ms.

Also measure the RESETCD time (low!) if the button is released.

The signal RESETCD must be low for 140ms ± 20ms.

IC7201 pin 28 RESETN; low time = 250 ms ± 20 ms

7.2.5.5 Check of microprocessor 68070.

Check after power on:
IC7201, pin 27 (= HALTN) = high (+5V)
IC7201, pin 28 (= RESETN) = high (+5V)
IC7201, pin 24 (=DTACKN) = changing high/low
IC7201, pin 26 (=BERRN) = high (+5V)

7.2.5.6 Low level test

Purpose is to test the hardware with software. Connect a terminal, or Service PCB to the UART of microprocessor 68070 via connector at rear side port 2 (= BU-2). How to start the low level test see section 5.1.

Settings of the terminal:

Baudrate: 9600
start bit: 1
data bists: 8
stop bits: 0
no parity/ no handshake

V 14410

Philips Consumer Service GmbH

Colonia-Allee 11, 51067 Köln

Tel.: 0221/96960-0, Fax: 0221/96960-809



PHILIPS

Art Code	AC 19	SI	Wichtig für die Werkstatt
Stichwort	CDI		Nummer
Memo	DE10B(6D)	Datum	13.05.1996

Service Information

Betrifft: Vorführ- Mode

Verteiler: F1, S4

Alle CDI- Player mit Schublade.

Diese CDI- Player sind mit einem Vorführ- Mode ausgestattet. Kunden können diesen Mode unbewußt mit gleichzeitigem halten der STOP- Taste beim Einschalten aktivieren. Hiernach ist ein öffnen der Schublade zum entfernen der CD- Platte nicht mehr möglich. Durch erneutes Einschalten mit gedrückter STOP- Taste wird dieser Mode wieder deaktiviert.

Bei entsprechender Beanstandung den Kunden bitte mit beiliegendem Hinweis informieren.

4822 830 19004



Werter Kunde !

Ihr CD-i Player war in den Verkaufs-Vorführ-Mode geschaltet. In dieser Vorführstellung kann die CD-Lade nicht geöffnet werden, damit bei Demonstrationen, z.B. bei Ausstellungen, in Geschäften und bei Händlern, die CD von Kunden nicht entnommen werden kann.

Wenn sich die CD-Lade bei Ihrem Gerät zu Hause nicht öffnen läßt und im Bildschirm-Menü das 'OPEN-ICON' Feld fehlt, ist der Vorführ-Mode aktiviert.

Beachten Sie bitte folgenden Bedienhinweis:

Um den CD-i Player wieder in die normale OPEN/CLOSE-Funktion zu schalten, muß der Verkaufs-Vorführ-Mode durch nachfolgende Bedienungsschritte de-aktiviert werden:

- A.) **Schalten Sie den CD-i Player mit der ON/OFF-Taste aus.**
- B.) **Halten Sie beim Einschalten die STOP-Taste gedrückt.**

Ob der Vorführ-Mode erfolgreich ausgeschaltet wurde, erkennen Sie im Bildschirm-Menü durch das Erscheinen des 'OPEN-ICON' Feldes.

Die Aktivierung des Vorführ-Modus ist wieder mit den gleichen Bedienschritten A und B möglich.



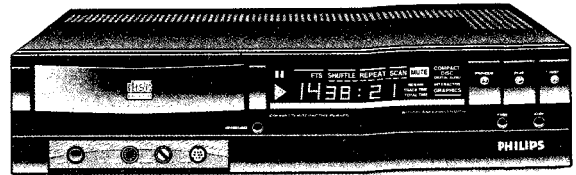
PHILIPS

COMPACT DISC INTERACTIVE PLAYER CDI 205

Service
Service
Service

Interactive
Media
Systems

CD-I



CDI 205

Circuit Description

COMPACT
disc
Interactive

CONTENTS

- 1 INTRODUCTION TO COMPACT DISC INTERACTIVE
- 2 CD-I THEORY OF OPERATION
3. EXPLANATION OF THE CDI205 PLAYER

CLASS 1
LASER PRODUCT

19 22 110 0420



PHILIPS

PCS 62533

<u>SECTION</u>	<u>DESCRIPTION</u>	<u>SECTION</u>	<u>DESCRIPTION</u>
1	INTRODUCTION TO COMPACT DISC INTERACTIVE	3.5	The Multi Media Controller (MMC) part
1.1	CD-DA discs	3.5.1	Systemcontrol
1.2	CD-ROM discs	3.5.1.1	Master C.P.U.
1.3	CD-I discs	3.5.1.2	Slave C.P.U.
1.4	User Shells	3.5.1.3	Sytem ROM
2	CD-I THEORY OF OPERATION	3.5.1.3.1	CD-RTOS software
2.1	Audio Formats	3.5.1.4	NV-Ram + Timer Clock
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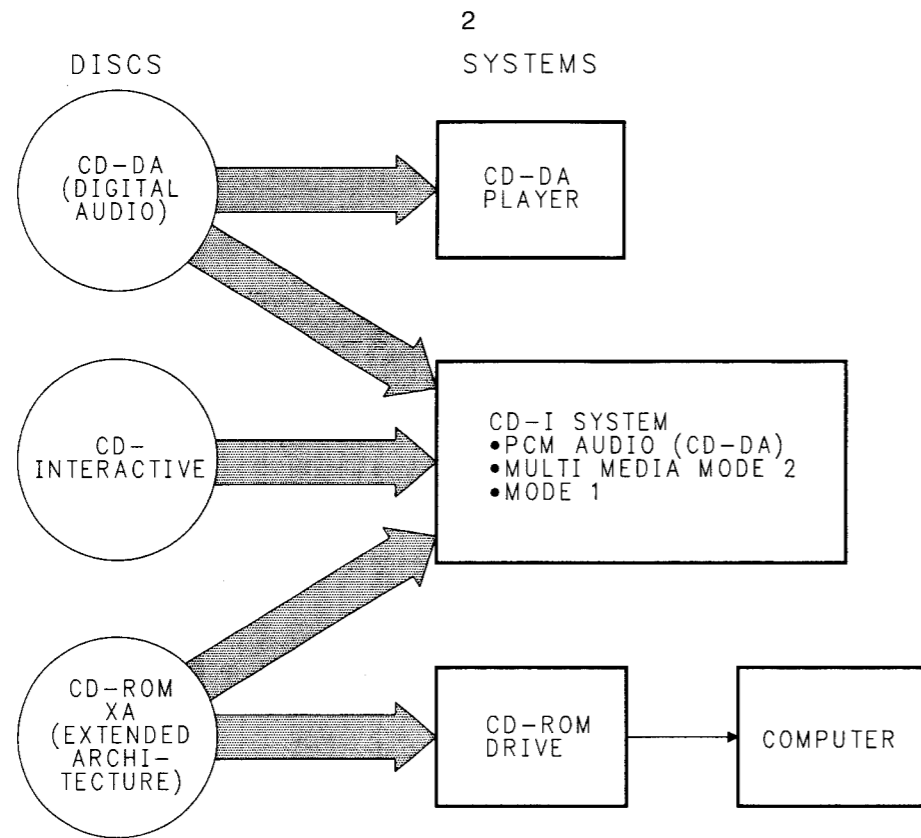


Figure 1 - Compact Disc Compatibility

1 INTRODUCTION TO COMPACT DISC INTERACTIVE

The introduction of the Laservision player has led to a host of devices that use a laser beam to read analog or digital optical recordings (Compact Disc, CD-ROM, CD-Video). The latest of such devices is the CD-I (Compact Disc-Interactive) player (see cover photo). As the name implies, the CD-I player basically uses the Compact Disc format and expands on this format with Interactivity. The CD-I player also lead to the development of expanded forms of formatting information placed on the disc (therefore the need for additional decoding methods). The CD-I player is also compatible with existing CD formats, such as the standard Digital Audio CD (CD-DA) and Photo CD (CD-ROM XA).

There are both commercial and consumer applications for CD-I. CD-I applications include education (interactive training), entertainment (games), information, and reference. The CD-I operating system is the Compact Disc — Real Time Operating System (CD-RTOS), based on the OS-9 operating system. CD-I software enables synchronization of Audio and Video information due to the interleaving of digital audio and video data on the disc. CD-I may combine audio, video (stills or moving), and text in a single application. For example, a CD-I application may have a narration (audio) along with text on the screen while a picture (video) is displayed on the monitor (standard TV monitor).

Or, another application may use animation in sync with the audio. CD-I also allows for the selection of one of several languages (application dependant). For example, a disc may include selectable narration in

English, French, Japanese, and Spanish. CD-I player operation depends on the application and type of disc. All Compact Discs have some common features, including error correction, interleaving, EFM (Eight-to-Fourteen Modulation), and a capacity of storing up to 650MB of digital information. Figure 1 illustrates the compatibility of each disc type.

1.1 CD-DA discs

The most familiar and popular is the standard **Compact Disc-Digital Audio (CD-DA)**. The Compact Disc is recorded to provide High Fidelity with virtually no distortion or noise. The CD-DA format is the basis for all other CD formats. CD-DA makes use of 16-bit PCM (Pulse Code Modulation) to place data on disc. In the encoding process, the analog audio is converted to 16 bits per channel at a sample rate of 44.1kHz. Each 16 bit sample is then divided down to an eight-bit symbol.

The CD-DA encoding process (see Figure 2) arranges six stereo sample periods of 192 bits or 24 bytes (6 samples times 32 bits or 4 bytes for right and left audio) into a frame (also known as a Small Frame). A Control and Display code (subcode data), parity codes, merging bits, EFM, and a sync code are all applied to the six stereo samples. Thus, a CD-DA small frame consists of 588 bits. This results in a frame frequency of 7.35kHz and a bit clock frequency of 4.3218 mega-bits per second.

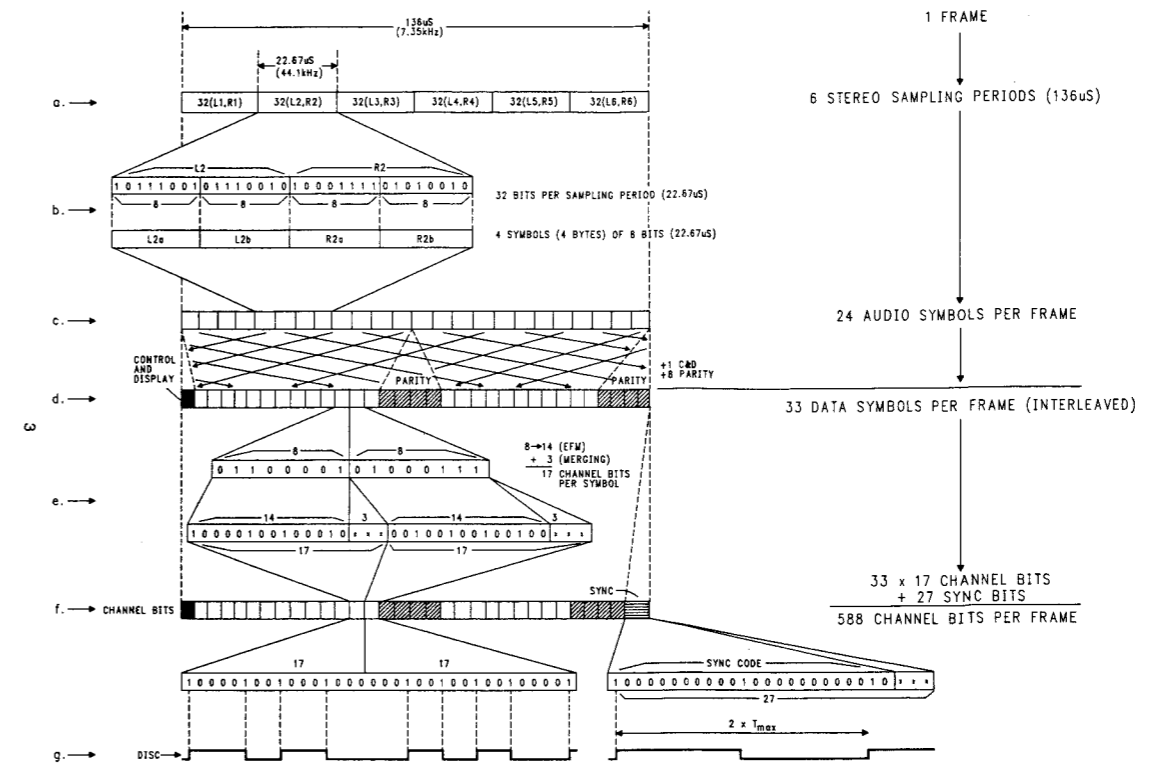


Figure 2 - CD Frame Format

	BIT POSITION 1								BIT POSITION 8
SUCCESSIVE 'SMALL FRAMES'	P	Q	R	S	T	U	V	W	
1	SUBCODE SYNC PATTERN S0								SUBCODE FRAME DURATION = 13.3ms
2	SUBCODE SYNC PATTERN S1								
3	¹ OR ₀	¹ OR ₀	0	0	0	0	0	0	SUBCODE FRAME REPETITION RATE = 75Hz
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	
97	¹ OR ₀	¹ OR ₀	0	0	0	0	0	0	
98	¹ OR ₀	¹ OR ₀	0	0	0	0	0	0	

Figure 3 - Subcode Frame Format

S0,S1	CONTROL	ADR	MNR	POINT	MIN	SEC	FRAME	ZERO	PMIN	PSEC	PFRAME	CRC
2 BITS	4 BITS	4 BITS	72 DATA BITS									16 BITS

a. DURING LEAD-IN TRACK(TOC)

S0,S1	CONTROL	ADR	MNR	INDEX	MIN	SEC	FRAME	ZERO	AMIN	ASEC	AFRAME	CRC
2 BITS	4 BITS	4 BITS	72 DATA BITS									16 BITS

Figure 4 - Q-Channel Format

Ninety-eight small frames make up a Large Frame or Subcode Frame (see Figure 3). The subcode repetition rate is 75Hz. The Subcode Frame is equivalent to a CD-ROM sector, which contains 2352 Bytes of data (98 small frames times 24 Bytes). The subcode is necessary to provide the CD player with information such as elapsed time and control data (see Figure 4). There are eight channels used in the Frame format, labeled "P" through "W". Until now, only the P and Q channels have been used. The other channels, R-W, can now be used for graphics and text. Compact Discs with graphics are known as CD+G. Until now, only the P and Q channels have been used. The other channels, R-W, can now be used for graphics and text. Compact Discs with graphics are known as CD+G. The lead-in track contains the Table Of Contents (TOC) information, incorporated in the Q-channel. The CD-DA format specifications limit the total playing time to 72 minutes of HI-FI stereo.

1.2 CD-ROM discs

Another type of disc is the **CD-ROM (Compact Disc - Read Only Memory)**. A CD-ROM disc contains over 600 mega-bytes of storage capacity for programs, data, and graphics. This storage capacity makes the CD-ROM advantageous for storage of large databases and program packages. However, CD-ROM discs are hardware dependent, as in any computer software. CD-ROM software, including programs and data, is thus developed for specific computer systems. Since programs are hardware dependant, the CD-I player does not run CD-ROM programs designed for computers. Generally, the CD-I player is also not designed to read data (graphics or text) from CD-ROM. A CD-ROM format which can be read by the CD-I player is **CD-ROM XA (Extended Architecture)**. One such application for CD-ROM XA is the Photo-CD. The Photo-CD can store up to 100 high resolution photos on a single disc.

CD-ROM defines data in the form of sectors. Each sector contains 2352 bytes of information and is recorded using the same EFM (Eight-to-Fourteen Modulation) technique used in CD-DA. EFM provides a first level of error protection well suited to audio data as well as binary data in general.

The sector contains synchronization, address and mode information. In addition, a sector contains a user data area of either 2048 bytes for Mode 1 or 2336 bytes for Mode 2 (See Figure 5). The difference between these two modes is that Mode 1 uses 288 bytes to provide an additional level of error detection (ED) and error correction (EC). This ensures a level of data integrity essential for critical information that does not degrade gracefully, such as text and binary data typically contained in databases. Mode 2 trades this benefit of additional data security for a maximum data transfer rate by making the additional 288 byte area available as user data. In this case the EFM is adequate for error protection of data such as video and audio encoded information that degrade gracefully.

The standard CD Table of Contents (TOC), although not available to the computer program, may be used by the CD-ROM player to locate a requested track. The TOC appears in the Q channel in the lead-in area of each disc. There are two types of tracks that the TOC can identify as stored on a CD-ROM disc: CD Digital Audio tracks, and data tracks.

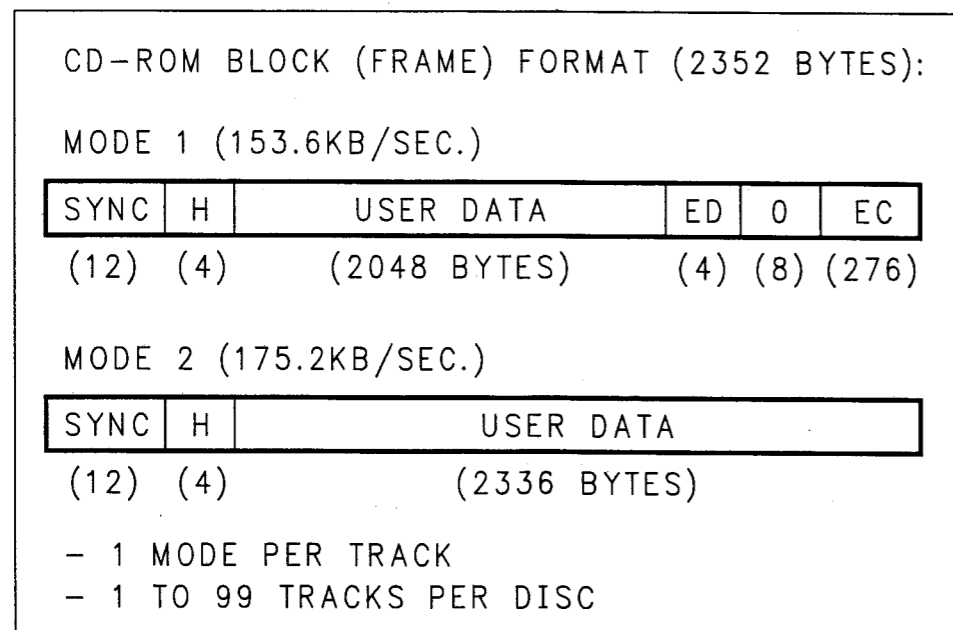


Figure 5 - CD-ROM Sector

1.3 CD-I discs

CD-I discs specifically meets the needs and requirements of the CD-I player. Since CD-I information may include audio, video, text, and program data, several different encoding methods are used (Video and Audio encoding methods are covered in the CD-I Theory of Operation section). Encoding standards are established for CD-DA, CD-ROM, and CD-I. Formats may be mixed on the disc, but Track One must always identify the disc as CD-I.

As with CD-ROM, CD-I defines data in the form of sectors, each sector contains 2352 bytes (see Figure 6). The CD-I physical format is based on CD-ROM, Mode 2. CD-I is primarily an audio/video driven medium. Thus, video must be synchronized to the audio with the CD data rate of 75 sectors per second. At the same time, there is a need for real-time interactivity. Thus all three data types, audio, video, and text (binary data), are physically interleaved. The sub-header (SH) mechanism is used for real time physical interleaving of data.

The two forms define two levels of data integrity. Some data degrades gracefully, such as audio and video. Whereas, text does not degrade gracefully.

Text is either present or not. Maximum bandwidth is the main requirement for audio and video information, whereas an extra layer of error correction is required for text. Thus there is a need for two different formats in Mode 2 for CD-I, Form 1 and Form 2.

The first of the two physical formats, Form 1, is tuned to the needs of text, computer data and highly compressed visual data. Thus, Form 1 uses 280 bytes for additional error correction (Error Detecting Code or EDC and Error Correcting Code or ECC), leaving 2048 Bytes as user data. The second physical format, Form 2, is used to fill the requirements of real time audio and visual data, leaving 2324 bytes of user data plus 4 bytes of reserved data.

The CD player is designed for varying the rotational speed to ensure a constant linear velocity at the readout head, resulting in a constant data transfer rate (frame rate) of 75 sectors per second. The resulting data transfer rates are 153.6KB/s for Form 1 and 174.6KB/s for Form 2.

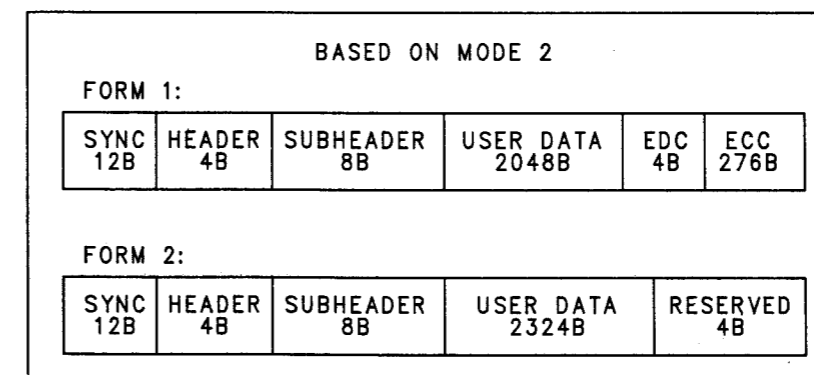


Figure 6 - CD-I Forms

1.4 User Shells

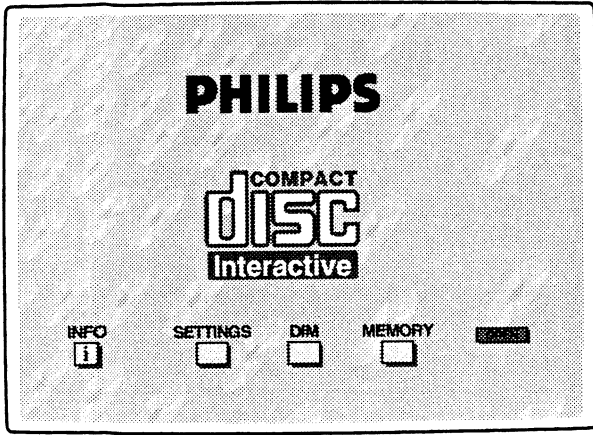


Figure 7 - Start-up Screen (size 3-1/4 x 2-3/8)

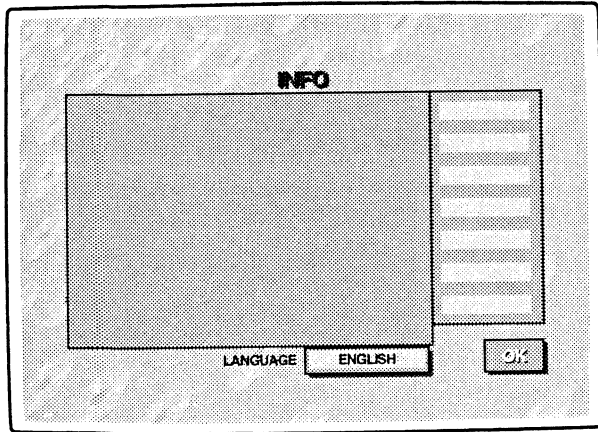


Figure 8 - Help Screen (size 3-1/4 x 2-3/8)

A Start-up Screen (Figure 7) is displayed when the player is turned On without a disc. The IR remote control or other pointing device, such as a mouse, is used to make screen selections. A selection is made by placing the arrow cursor over a command icon and pressing the Activate Key (one of the keys around the joystick). Alternately, dedicated keys, such as the Play or Open Keys, may be used to perform player functions. Other screens are accessed from the Start-up Screen, including the Info Screen (Help), Memory Screen and Settings Screen. Selecting the Info Icon brings up a help screen (see Figure 8). The help screen displayed is dependent on the type of disc that is currently loaded in the player. If no disc is present, the help screen displays a message about loading a disc.

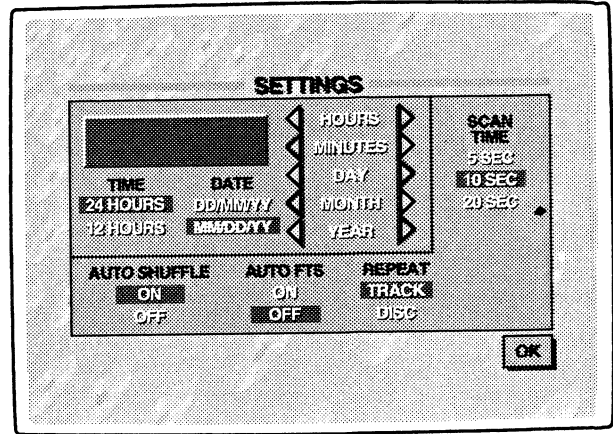


Figure 9 - Settings Screen (size 3-1/4 x 2-3/8)

The Settings Screen (Figure 9) allows a user to set the date and time, as well as selecting options regarding the playing of discs. For example, the user may choose to turn the Auto Shuffle option On. Then, the Auto Shuffle option is active any time a CD-DA is loaded into the player.

2 CD-I THEORY OF OPERATION

2.1 Audio Formats

The audio formats are illustrated in Chart 1. There are four forms of Audio formats which may be applied to CD-I. The first is the familiar CD-DA. The standardized format for encoding CD-DA as Pulse Code Modulation (PCM) includes the 44.1kHz Sampling Frequency (fS) and 16 Bit sampling (Significance). This results in a dynamic range of greater than 90db with a bandwidth (BW) of 20kHz and a maximum playing time of 72 minutes of Hi-Fi stereo audio.

Besides the normal CD-DA information, the audio data coding used in CD-I is 8 or 4-bit Adaptive Delta Pulse Code Modulation (ADPCM). A lower data rate (8-bit instead of 16-bit) with a lower sampling rate and a different coding technique is used since no more than 50% of the time is allocated for audio information. The Adaptive Delta PCM (ADPCM) coding technique used to store audio information more efficiently, requires additional processing beyond 16-bit PCM for both encoding and decoding.

The chart shows the specifications for each level. The level used depends on the application. For example, to provide maximum time where high fidelity is unnecessary, such as a narration, Level C is used. Using this level limits the frequency response to 8.5kHz, but allows up to approximately 19 hours¹ (with no other format: video, CD-DA, text) of mono audio or 9½ hours stereo on a single disc.

Level A is comparable to High Fidelity from an LP record with a bandwidth of about 17kHz and Level B is comparable to FM broadcast audio.

1. A channel is equivalent to a maximum of about 72 minutes continuous playing time. The "19 hours" are composed of 16 parallel channels of some 72 minutes each, with a 1 to 3 second gap before the next continuous "hour" can be listened to..

Both Levels A and B are suitable for music, although the bandwidth and significance are not as good as CD-DA. Level C limits the bandwidth to only 8.5kHz and is therefore unsuitable for music.

By using the three levels of ADPCM, information other than audio (video, text, and program) can be included on a disc, while still allowing 72 minutes of audio, as illustrated in Figure 17. The CD Information Intensity Chart shows the percentage of data which can be allotted for non-audio data for each level as compared to CD-DA. Thus, 100% of a CD-DA disc is used when 72 minutes of audio is encoded onto the disc. Whereas, if the same 72 minutes is encoded using ADPCM Level A, only 50% of the disc is used for audio, leaving 50% for non-audio data. Likewise, Level B allows 25% for 72 minutes of audio and 75% for non-audio data. Level C allows 6% for audio and 94% for non-audio data.

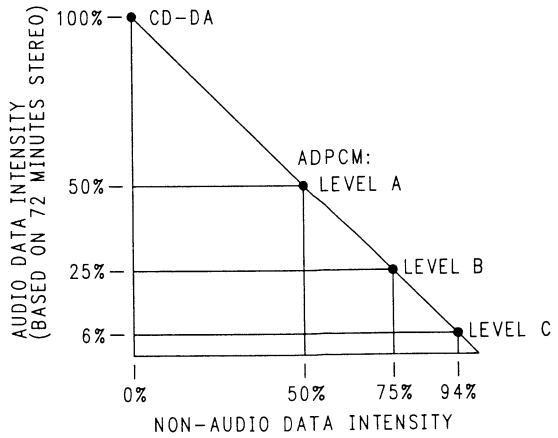


Figure 17 - CD Information Intensity Chart

FORMAT						
	fS IN KHZ	SIGNI- FICANCE	BW IN KHZ	CHANNELS	XSYS IN MHZ	t MAX IN MIN STEREO (MONO)
CD-DA (PCM)	44.1	16	20	1 STEREO	11.2896	72
LEVEL A (AD-PCM)	37.8	8	17	2 STEREO 4 MONO	9.6768	144 (288)
LEVEL B (AD-PCM)	37.8	4	17	4 STEREO 8 MONO	9.6768	288 (576)
LEVEL C (AD-PCM)	18.9	4	8.5	8 STEREO 16 MONO	4.8384	576 (1152)

Chart 1 - CD-I Audio Formats

2.2 Video Formats

Since there are several television systems used around the world (see Chart 2), the video encoding system for CD-I allows for a world-wide standard. That is, the video data can be decoded to play on NTSC, PAL, or SECAM television systems. Besides the various audio quality levels, there is a need for various video quality levels. The video quality levels offer a choice of resolution and picture type (encoding process).

CD-I VIDEO FORMATS:

- **WORLD-WIDE FORMAT**
-NTSC, PAL, AND SECAM
- **THREE RESOLUTION MODES**
- **THREE PICTURE TYPES**

(ENCODING METHODS)

The resolution modes provide for both present and future television systems (see Chart 3). The three modes are Normal, Double or Enhanced, and High resolution. The chart shows the three modes with their respective horizontal and vertical lines of resolution for all three television standards.

The picture code depends on the type of picture to be displayed. Chart 4 compares each type of coding system. Picture coding provides for three picture qualities: natural pictures and two graphics modes. Natural stills are best handled by YUV² coding for an equivalent of 24-bit color depth.

2. See YUV Encoding in the glossary.

RESOLUTION	PAL 625 LINES
NORMAL	384X280 PIXELS
DOUBLE	768X280 PIXELS
HIGH	768X560 PIXELS

Chart 3 - Video Resolution Modes

FORMAT	APPLICATION	MEMORY	COLORS
DYUV	NATURAL STILLS	105kB/PICTURE	16 Million
CLUT	GRAPHICS ANIMATION	105kB/PICTURE	256 of 16 Million
RGB	COMPLEX GRAPHICS	210kB/PICTURE	32,768
RUNLENGTH	ANIMATION	AT LEAST 10-FOLD SAVING	128

Chart 4 - Picture Types (Encoding Process)

Quality graphics are best handled by Color Look-up Tables (CLUT's), or by absolute RGB coding for user manipulated graphics. Compression techniques are required to provide full screen animation. Natural pictures, using YUV (Y, R-Y, and B-Y) coding, occupy about 325kB per picture without interlacing (650kB with interlacing). To decrease throughput times and maintain a high quality image, all natural pictures are compressed with DYUV (Delta YUV) coding. DYUV reduces the memory requirements to 108kB. Thus, the DYUV coding system provides a transfer rate of one full-frame in about 0.6 seconds at a data rate of 174.6kB/s (Form 2).

The CLUT (Color Look-Up Table) mode is best used for graphics animation. CLUT can be used as 8 bits out of 243 bits (for 256 colors out of 16 million), requiring 108kB of storage capacity per picture. Compression can reduce this to less than 10kB per picture. CLUT with compression provides full-screen animation with the interleaving of pictures and sound. A picture refresh rate of 17 frames per second is achievable in Form 2.

The other graphics mode is based on absolute RGB coding and is best applied to user manipulated graphics³. Fifteen bit RGB graphics (32,768 colors) produce exceptionally crisp pictures at a cost of about 215kB per picture. No compression is used in this encoding system.

3. Example: user manipulated graphics allows the user to change colors in a picture. This may be applied to games or educational applications.

2.3 Text Coding

Text encoding may be handled using two basic methods, by a bit map process⁴ or with character encoding (see Figure 18). The bit-map process requires five bytes for each character. This limits the number of characters to a maximum of 120 million per disc, if only 16 colors are used in an 8 x 10 matrix of any shape

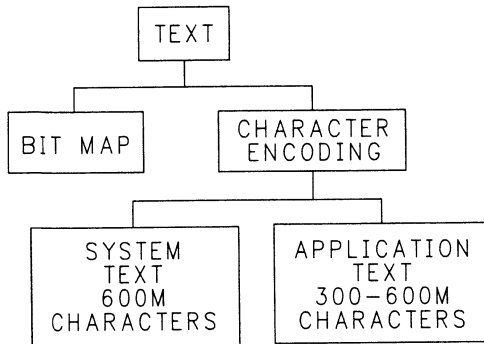


Figure 18 - Text Coding

4. The bit-map process may be with or without data compression (CLUT plus compression techniques).

Character encoded text can be system text or application text. The standard character encoded text (system text), using one byte per character, allows 600 million characters in a full disc. Application text is encoded with two bytes per character. The second byte specifies factors like color, font type, and size. This extended coding method allows 300 to 600 million characters per disc. Character coding allows interactive manipulation of text. For example, the user may incorporate part of the text from the disc into another document.

There is a need to limit the number of characters on screen due to the limited resolution of a normal TV. Thus, text is limited to 40 characters on 20 lines. The characters are contained in a safety area of 320 x 210 76 pixels in the center of the screen. With the high resolution screens used in computer monitors and future high definition or digital TV's, the High Resolution mode allows 80 characters to be presented on up to 40 lines. The safety area for the High Resolution mode is 640 x 420 pixels. The text is only stored once since compatibility between the two resolution modes is maintained.

2.4 Video Effects

A wide range of visual effects are provided in the CD-I system, including: wipes, cuts, scrolls, overlays, dissolves and fades. Up to five overlaying video planes are provided, with both transparency and translucency for all except the background planes. One plane is reserved for external video and another for the cursor.

2.5 Decoding Process

The system must have the ability to decode information stamped on the disc. In the standard CD-DA, this is straight-forward since there is only one type of encoding method. CD-I discs use more than one type of encoding process and include audio, video, and text information. The Digital information, once read from the disc, must be routed to the correct decoding circuits to be converted to their respective analog signals, whether audio, video, or text.

2.6 Microprocessor and Operating System

The CD-I software (discs) includes more than just the video, text, and audio information. The disc also provides instructions (application program) to the CD-I player (program). In addition, there is a need to provide real time operation in applications such as entertainment and education. Real time applications require machine language (from the disc) to execute specific tasks. All machine language sets are specific to a microprocessor family. Specifying the microprocessor family and operating system makes it possible to produce discs carrying audio, video, text, binary data and application programs that will work on all CD-I players from all manufacturers. The microprocessor family specified for CD-I is based on the Motorola 68000 family. The Philips CDI910, CDI601 and CDI602 use the MC68070 microprocessor.

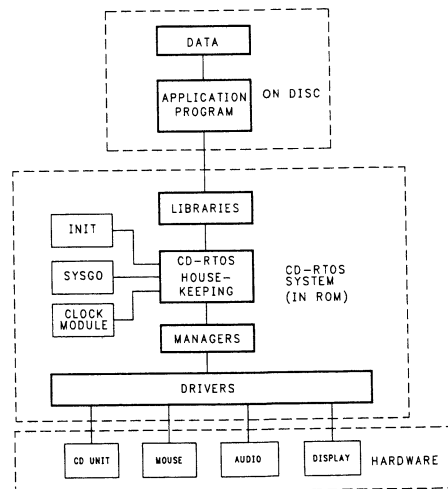


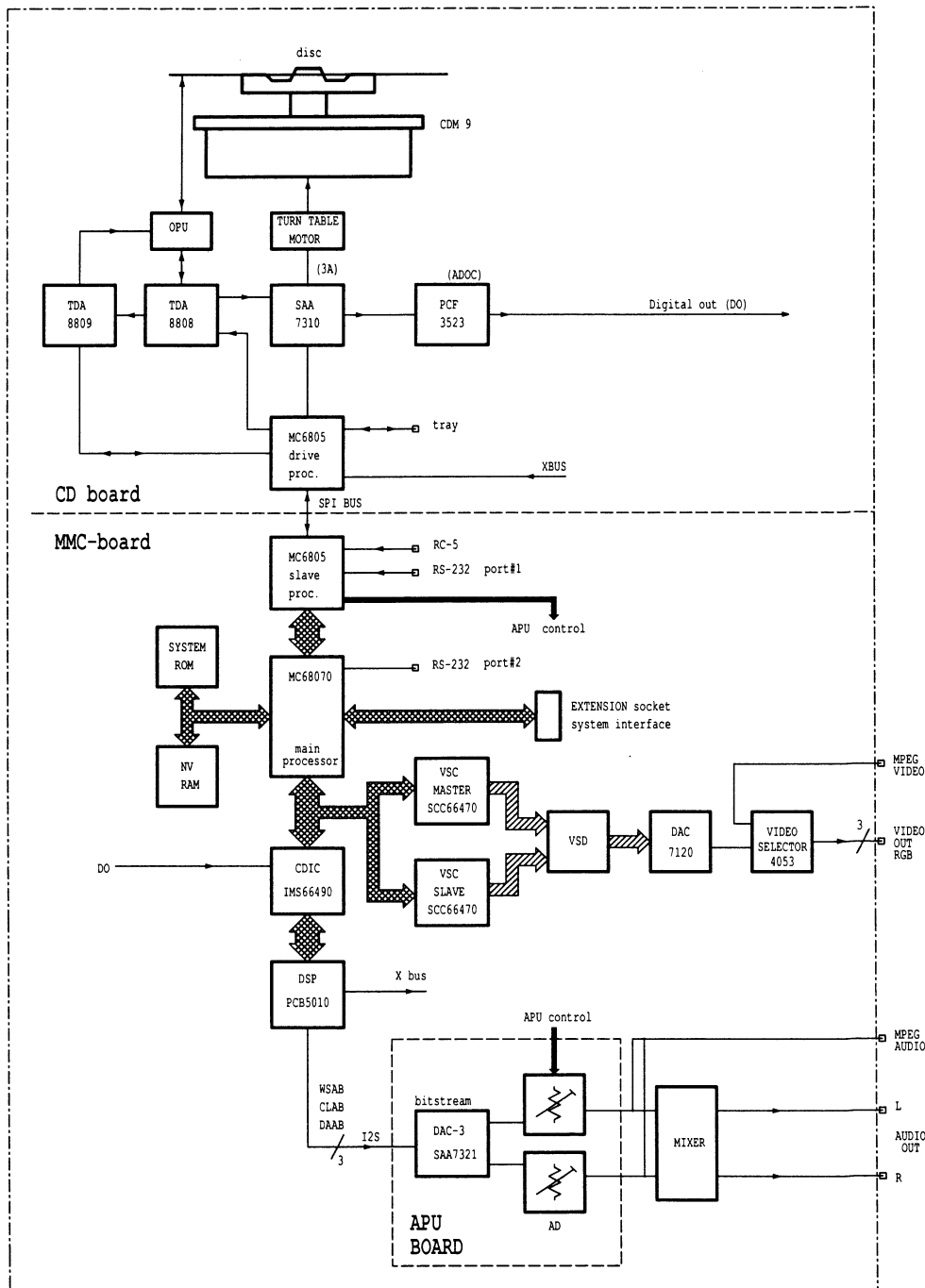
Figure 19 - CD-RTOS Organization

The Compact Disc Real Time Operating System (CD-RTOS) used in CD-I is based on the OS-9 real time operating system⁵ (see Figure 19). A series of instructions (CD-RTOS) is loaded from ROM into memory (booted) to create the user shell⁶ and load the operating system libraries, managers and drivers when the player is turned On. The user shell along with the peripheral devices, such as the mouse or the remote control, allows the user to interface with the system hardware and software.

5. CD-RTOS is customized to fit the needs of the CD-I system.

6. The player shell is dependent on the software or type of disc (CD-DA, CD-I) and whether there is a disc loaded in the player.

Fig.1 BLOCKDIAGRAM



3. EXPLANATION OF THE CDI205 PLAYER

A rough blockdiagram of the player is shown in figure 1.

The player is build up with 2 boards : the CD board with the drive processor, the servo ic's, the optical pick-up unit and a MMC (Multi Media Controller) board with the MC68070 processor (item 7201 on MMC panel) , the slave processor (item 7206 on MMC panel), the DSP (Digital Signal Processor, item 7306) , the CDIC (Compact Disc IC, item 7301) and the video ic's VSC and VSR.

3.1 CD Part

The CD board reads the high frequent signal from the disc, transforms it to digital out (DO) which is sent to the MMC board. The DO signal goes to the CDIC. Together with the DSP the DO signal is split into a video signal, going to the video ic's and into an audio signal (I2S format) going to the APU. The video ic's convert the signal to RGB, the APU translates the audio signal to analog audio.

The master processor in the CDI player is the MC68070 processor, it controls and manages all the signals from or to the player.

The 'slave' processor receives RC-5 and RS-232 signals and send these signals to the MC68070 processor. The slave processor has therefore a direct access to the MC68070 bus. Another part of its job is to send control signals to the APU (Audio Processing Unit), which manages the MUTE signal and the different amplifier ranges of the audio. Furthermore, the slave has a direct link to the other MC6805 processor (the drive processor) via the serial peripheral interface (SPI-bus). It is through this bus that service commands from the MC68070 are send to the drive processor. Error messages and status information from the drive processor are send over the SPI-bus to the MC68070 processor. So, the SPI-bus makes a bidirectional communication possible between the MC68070 and the drive processor.

3.1.1 The Loader

The loading consist of :

- * a loader system, which uses a tray for inserting the disc. Detection of loading or ejecting a disc is done with the tray switch (item 10 of the exploded view)
- * an optical pick-up mechanism with DC-motor, type CDM9. The CDM9 is a swingarm reading mechanism, incorporating the unique integrated one-spot light pen the LGDU (Laser Detector Grating Unit).

Output signals :

- **D1 - D4.** LF signals for generation of Focus Error (FE) and Radial Error (RE1, RE2).
- **HF,** containing the coded data from the disc, EFM.
- **LM.** The Laser Monitor signal to control the intensity of the laserlight.
- **TRAY SWITCH.** tray switch signal.

Inputs signals :

- **LO.** The Laser On signal from the lasersupply circuit.
- **Vc** Signal for the DC-turntablemotor.
- **TMOU** Tray motor control signal

3.1.2 The Drive Processor

The drive processor controls all the disc accesses. It receives disc-access commands (like jump to an absolute time, pause, stop, read-toc,...) from the MC68070 via the DSP (digital signal processor), moves the optical pick-up to the correct position on the disc and gives a signal when the data from the disc is (in)correct.

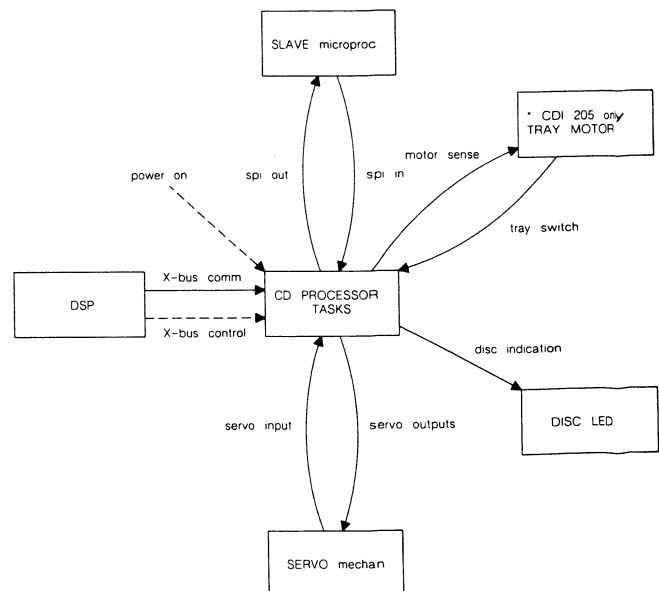
Inputs signals :

- X-bus commands from the DSP
- commands from the slave processor
- inputs from the servo ic's

Outputs signals :

- messages to the slave processor
- disc indication LED
- signals to the servo ic's.

Fig. 2 shows in- and outputs in a diagram.



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Fig. 2 : drive processor context diagram

Micro processor MC68HSC05C8 (ITEM 7201 ON CD PANEL)

ABBREVIATION	PIN NBR	DESCRIPTION
VDD	40	Supply voltage input 5V.
OSC1	39	Oscillator input 1.
OSC2	38	Oscillator input 2.
TCAP	37	Timer Capture interrupt line
TL	36	Track Lost signal
TCMP	35	Timer Compare output
SPISS	34	Serial PeripheralInterface Slave
SCK	33	Serial Clock
MOSI	32	Master Out Slave In
MISO	31	Master In Slave Out
REDIG	30	Radial Error digital
MC	29	Motor Control signal
COXN	28	X-bus Clock
SOXENN	27	X-bus Serial Output enable LOW-active
COC	26	Command Control.
V-FLAG	25	Error flag
SOXRQN	24	Serial Output Request line
DIV4	23	Divide by 4
DOXN	22	Data Out line
CADDYSW.	21	Caddy switch detection.
VSS	20	Power supply ground input.
SPISS	19	SPI Slave Select line
MUTE	18	Soft mute
TRAY	17	Tray Motor On/Off
QCL	16	Q channel clock
CADDY-IN	15	Caddy busy indication signal
QRA	14	Q data Request
QDA	13	Q data line
AM	12	Additional Mute
IDAC	11	1 bit DAC correction signal
BO - B3	10 - 7	DAC/control of Radial processor.
SWAB/SSM	6	Start/Stop signal for Turntable motor
SI/RD	5	Start Initialization Focus / startready
CRI/DODS	4	Counter Reset Inhibit / Drop Out Detection
	3	Suppression not connected
TRQ	2	not used
RESETCD	1	Reset input

To transform the given inputs to the desired output, the drive processor has several software modules.

start and play :

* input :X-bus commands, subcod time and servo information
 * action:this function does all the necessary actions to start up the player (from stop position) and to keep the player in the normal play mode.

jump to a given time :

* input :an X-bus command, subcod time and servo information.
 * action:this function jumps to a given absolute time on the disc.

pause :

* input :an X-bus command, subcode time and servo information.
 * output:when the pause command arrives, the absolute time at that moment is stored. Every main loop a check is done to control if the current absolute time is different from the stored one. If so, a jump to the stored time is done.

service :

* input :SPI commands and servo status information.
 * action:depending on the SPI commands, a service step is executed.

read subcode :

* input :servo status information
 * action:every 32 ms in the normal play mode, the subcode information from the 3A chip is read in.

stop :

* input :a X-bus command and servo information.
 * action:this function stops the player.

communication function :

* input :the hardware X-bus and SPI bus
 * action:this function reads the commands from the X- and SPI bus and set the necessary tasks to execute the command. Error messages and the drive status are send to the slave processor over the SPI bus.

3.1.3 The Communication Function**3.1.3.1 The X-bus routine**

To access the disc the MC68070 will send commands to the drive processor via the DSP. The DSP (PCB5010) has on board 2 standard serial data input and output busses. One of these output busses (the X-bus) is used for sending the commands to the drive processor.

The X-bus consists of 4 lines :

- SOXEN : SOC enable signal from an external device
 - 0 : enables SOC
 - 1 : disables SOC
- SOXRQN : SOC ready indicator for the external device
 - 0 : SOC ready to shift data out
 - 1 : SOC not-ready to shift
- DOX : serial data output
- COX : serial output clock from an external device

SOC = serial output control.

COX is an external clock (from the drive processor) that continuously must be present (frequency between 30 kHz and 100 kHz). When the DSP has a command ready, it sets the SOXRQN line low. When the drive processor sees that the SOXRQN is low, it sets the SOXEN line low. At that moment the command is clock out of the DSP at the falling edge of the clock (COX). Data is coming out of the DOX line.

A DSP command is always 32 bits long.

After 32 clock pulses the SOXRQN line becomes high and the drive processor then sets the SOXEN line high again indicating that the communication is completed.

An extra controller line, COC, indicates when the drive processor is executing the received command. COC low means that the drive processor is executing the command; when the command is executed, the drive processor makes COC high. During COC low, no commands from the DSP are read in. (The COC line is an interesting line for debug facilities : it indicates that there is still communication between the DSP and the drive processor; COC always low means that the drive can't execute the command he is still busy with executing the command, COC always high with COX present, means that the DSP has no command to send to the drive).

3.1.3.2 The X-bus commands

The X-bus command is 4 bytes long; the first byte is a command byte, the three other bytes give information depending on what the command is.

The commands are divide in 2 parts : commands concerning a CDI disc and commands concerning a CDDA disc.

CDI commands :

- C0 000000 : read toc command
- 36 000000 : stop the player
- 30 000000 : pause the player
- C1 000000 : continue playing (after pause)
- E0 ffssmm : current time min sec frames (BCD)
- E1 ffssmm : requested time min sec frames (BCD)

CDDA commands :

- 02 000000 : start the player
- 03 000000 : stop the player
- 05 000000 : pause the player
- 04 000000 : continue playing (after pause)
- 14 ffssmm : goto abs. time min sec frames (BCD)

3.1.3.3 Messages from and to the slave processor

A bidirectional communication between the MC68070 and the drive processor is necessary for the following reasons :

- service test for the CD panel.
- some information from the CD print must be send to the 68070 (like the caddy switch, error messages, CD status, software version number,...).

There is a communication bus between the MC68070 and the MC6805 slave processor. An extra communication link between the 2 MC6805 processors (via **the SPI bus :SCK, MOSI, MISO, SPISS**) makes the bidirectionary bus between the 68070 and the CD drive processor possible. See fig.5.

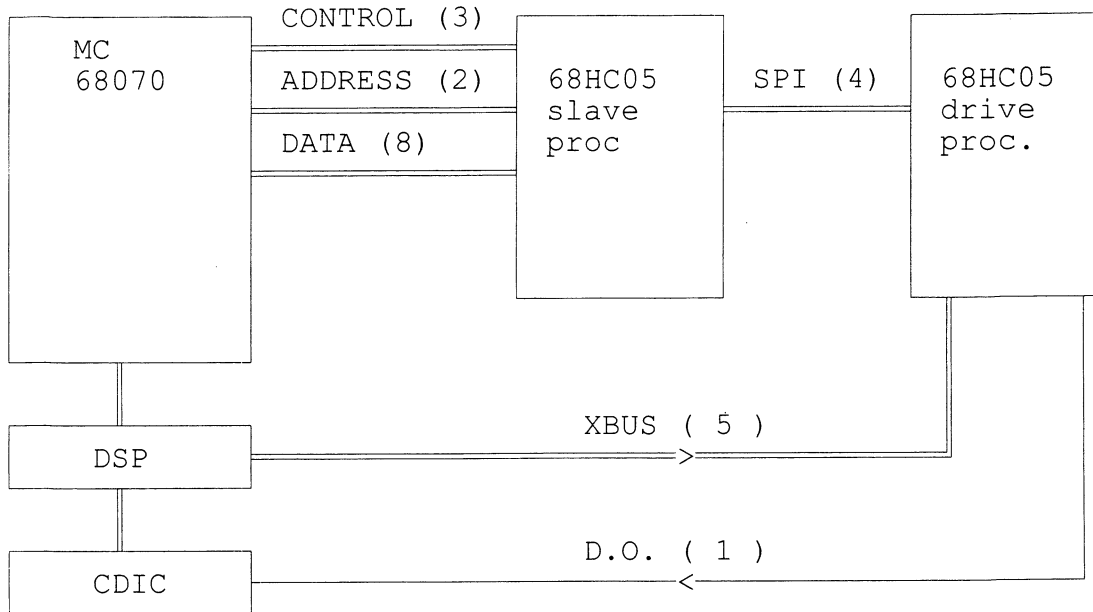


Fig. 5 : The communication between MC68070 and drive processor.

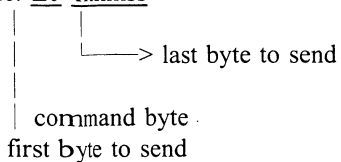
3.1.3.4 Internal Communication Data format

For the communication between the MC68070 and the drive processor, the slave processor is set in a 'transparent mode'. This means that the slave processor doesn't check the messages from the MC68070 or the drive processor if they are correct, it only sends the total message (4 bytes) through.

The format of the messages between the MC68070 and the drive processor is as follow :

- each message exists of 4 bytes : the first byte is always a command byte, the 3 last bytes are data bytes
- order of sending the bytes : the command byte is sent first, followed by the 3 data bytes

example: E0 ffmmss



- the MSB of the command byte (= first byte of a message) is 1, the MSB of the 3 data bytes is 0.

3.1.3.5 Data from 68070 to the CD drive processor

The following commands can be send from the MC68070 to the drive processor :

- A0 000000** : send CD status
- A1 000000** : send absolute time
- A2 000000** : send track/index
- A3 000000** : send software version number
- A4 000000** : send this command back to the 68070
- A5 000000** : send error messages
- AB xx0000** : service command

- xx = 55 : start service routine
- xx = AA : end service routine

3.1.3.6 Data from CD drive processor to slave processor

Commands send after a request :

A0 xxyy00 : see 6.4.b

A1 mmssff : absolute time (mm : amin, ss : asec, ff : afram in BCD)

A2 xxyy00 : track/index (xx = tracknumber yy = indexnumber in BCD)

A3 xxyy00 : software versionnumber (xx : high versionnumber yy : low versionnumber in BCD).

A4 xxyyzz : sends back the received command

A5 xx0000 : error messages

- xx = 2 : focus error
- xx = 3 : radial error
- xx = 5 : off error (TL stays low for 50 ms)
- xx = 6 : jump error
- xx = 7 : subcode error, no valid subcode in 3 s
- xx = 8 : TOC error : out of lead-in area while reading the TOC
- xx = 30 : to many grooves to jump
- xx = 31 : search time out
- xx = 32 : bin. search error
- xx = 33 : search index error
- xx = 34 : search time error
- xx = 37 : selection error

Commands send without a request :

The following commands are send to the MC68070 without a request from the MC68070.

B0 00 xx yy : disc information

- xx = 0 : cdda disc
- = 1 : cdrom disc
- = 2 : cdi disc
- = 3 : cdi disc + cdda

This information is send once after power on and after disc change.

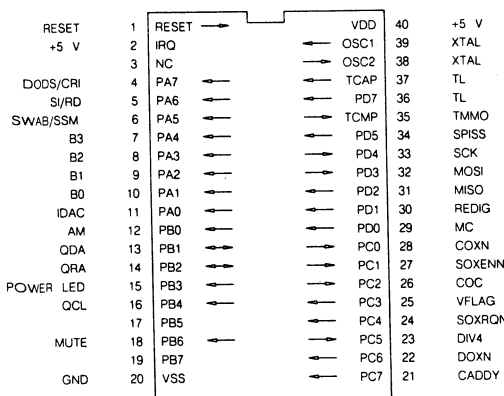
A0 xx 00 00 : status information

- xx = 13 : caddy switch active
- xx = 15 : the tray is open or is moving out.
- xx = 16 : the tray is closing.
- xx = 12 : no disc present.
- xx = 11 : the player is starting up.
- xx = 10 : the player is stopping.
- xx = 09 : the player is in the leadout.
- xx = 08 : the player is reading TOC.
- xx = 04 : the player reads data.
- xx = 03 : the player reads audio.
- xx = 01 : the player is searching to a given time.

- if bit 5 of xx = 1 : the player is in pause.
- 0 : the player is not in pause.
- if bit 6 of xx = 1 : 3" disc (bit 7 = 0)
- if bit 7 of xx = 1 : 5" disc (bit 6 = 0)
- if bit 6 en bit 7 of xx both = 0 : discdiameter unknown (no disc)
- remark : - the value of xx is decimal.
- the status is only send when the status is changed.

3.1.4 The Servo Software Control

Figure 6 shows the connection diagram of the drive processor. The meaning of each in- and output is explained below. For a good understanding of the servo function you have to take the electrical scheme of the CD board and it is interesting to read the spec's of the servo ic's TDA8808 and TDA8809.



MDA 02922

FIG.6 THE DRIVE PROCESSOR

The meaning of the used servo signals is as follows :
Si/RD :On/off control for the focus servo system. This line is continuously made low by the SERVO-μP during the stop condition. At starting up, the SERVO-μP forces this line in a high-Z state. In this case the focus servo system is enabled. After some time the Si/RD-signal is made low for a short period to indicate that the focus servo is ready.

TL :Track loss. This signal is made low by the TDA8808 as soon as a track is lost.

REdig :Digital radial error signal (Re2-Re1).

B0 :

B1 :Input control bits for off-, catch-, play-status and DAC

B2 :output-current for radial motor.

B3 :

DIV4 :Divide by 4 / fast select signal. As the DIV4 signal becomes low the REdig signal is divided by 4 and then redirected to the TL input on the SERVO-μP. This is necessary for obtaining an appropriate bandwidth for a fast jump (20kHz). When the DIV4 line goes high again the REdig signal becomes normal (not divided) and the TL output signal of the TDA8808 is redirected to the TL input of the SERVO-μP.

IDAC : ½ bit DAC. This signal is normally held high-Z by the SERVO-μP. However when TL goes low the CORR line can influence the proportional amplification of the radial servo (improved S-curve).

CRI :Counter reset inhibit. This signal goes low during a real track loss (>600μs) or during execution of a jump command. When low, this signal allows the divide-by-588 master counter in the DEMOD timing of the SAA7310 to run free. The signal becomes high during initialization of the "catch" status of the radial servo.

DODS :Drop-out detector suppression. This signal is externally hard wired with the CRI-signal.

QRA :

QDA :Subcode channel.

QCL :

SWAB/SSM :Subcoding word clock and start/stop turntable motor. This line is continuously made low by the SERVO-μP during the stop condition. At starting up the SERVO-μP forces this line to the high-Z state. In this case the turntable motor is started and the subcoding word clock is connected to this line by the SAA7310. If this line is forced low by the SERVO-μP, a motor stop condition will be decoded by the SAA7310 and fed to the turntable motor control logic circuit.

MC :Motor speed control. The SERVO-μP uses this line to measure the turntable motor starting up time. This is necessary for the 8cm/12cm disk identification and for the software controlled brake of the turntable motor.

AM :Additional mute. This signal goes low as soon as a real track-loss occurs or during execution of a jump command. When this signal is low, all data will be forced low at the pre-FIFO stage. The muted data will then be corrected after the de-interleaving. The AM- signal goes high together with the initialization of the "play"-status on the radial servo.

MUTE :Digital mute. This signal is made low by the SERVO- μ P as soon as a jump is done. During a jump, the disc information is not relevant for the MMC.

Remark:the lines B0...B3 controls the off-, catch-, play-status and DAC output-current for radial motor. The table below gives the truth table for the DAC output current.

func-tions	DAC outp	logical inputs				intern. switches		
		IREout/IDAC	B3	B2	B1	B0	lag	rad s/c
push	-1/2	0	0	0	0	off	off	on
(kick)	-2	0	0	0	1	off	off	off
OFF	0	0	0	1	0	off	off	on
OFF	0	0	0	1	1	on	off	off
PULL	1/2	0	1	0	0	off	off	on
(kick)	2	0	1	0	1	off	off	off
CATCH	0	0	1	1	0	off	on	on
PLAY	0	0	1	1	1	off	on	off
PUSH	-1/2	1	0	0	0	on	off	on
PUSH	-3/8	1	0	0	1	on	off	off
PUSH	-1/4	1	0	1	0	on	off	on
PUSH	-1/8	1	0	1	1	on	off	off
PULL	1/2	1	1	0	0	on	off	on
PULL	3/8	1	1	0	1	on	off	off
PULL	1/4	1	1	1	0	on	off	on
PULL	1/8	1	1	1	1	on	off	off

3.1.4.1 The main servo functions

The basic servo functions for the drive processor are :

- start up the player,
- play a part of the disc,
- jump to a given absolute time,
- pause the player,
- stop the player.

The servo software is also optimized to shock resistance and playability.

The next part of this document explains in a short way the starting up procedure, the jump routine and the stop procedure.

3.1.4.2 The start up procedure of the CD-part

Going from a 'stop' position to 'normal play' mode (starting up) happens in a few steps :

a. Pull the arm inside and start up the focus. Pulling the arm inside is done by setting $b3..b0 = + 25\mu A$. Starting the focus is done by making the line Si/RD high impedant. At that moment the focus procedure is done completely in hardware by the TDA8808. When the focus is found, the TDA8808 make the Si/RD line during a short time low. Because this signal is asynchronous, the servo software does not look at this puls (and does not know at this moment that the focus point is found).

b. Wait 400 ms to give the hardware the time to focus; enable TL interrupt.

c. Start up the turntable motor and look for 4 TL signals within 400ms. When there is no TL signal after 4 us, then the direction of the turntable motor is switched. The 4 TL pulses is a sign for the servo software that the optic is in focus. When there are no 4 TL signals during 400 ms, the start up procedure is restart again. If there are no 4 TL signals the second time, then the player is stopped (turntable motor off, laser off).

d. Wait 400 ms to start up the turntable motor.

e. Search for the point of minimum excentricity. First we look for 2 TL pulses with REDIG low; if we find them, then we look for 1 TL pulse with REDIG high. If this exists, then the point of minimum excentricity is found else an excentricity error is generated and the player is stopped. When there is no error, the player is set in catch mode : $b3..b0 = 0110$.

f. If there is no TL during 1.6 ms (the arm is on the groove) then goto play mode (g) else goto catch mode.

g. Play mode. The player is set in play mode ($b3..b0 = 0111$). This is the normal play mode. At this moment the digital audio or data is valid.

3.1.4.3 The search and jump procedure

The jump commands from the X-bus are always jumps to an absolute time on the disc. There are 2 modules that controls a jump to an absolute time from position A to B.

1. The search module : calculates the difference between position A and B. This time is converted into seconds and frames. With a table, that contains the number of grooves per second for a position on the disc, the total number of grooves between A and B are calculated. This number of grooves has to be jumped and is transferred to the jump routine. After a jump a check is done if the current absolute time is the asked time of position B. If there is a difference the search procedure is restarted until the desired position is reached else there is a timeout.

2. The jump module : jumps the given number of grooves. Basically there are 2 different jumps := 1 groove jump and > 1 groove jump.

The **1 groove jump** is used when the number of grooves are less than 5 (so when 5 grooves have to be jump the player jumps 5 times 1 groove) and in the PAUSE mode.

When there are **more than 5 grooves to be jump** the DAC current is depending the number of grooves. In fact the move of the radial arm is always controlled and the DAC current will be adapted during the jump, depending on the number that still has to be jumped.

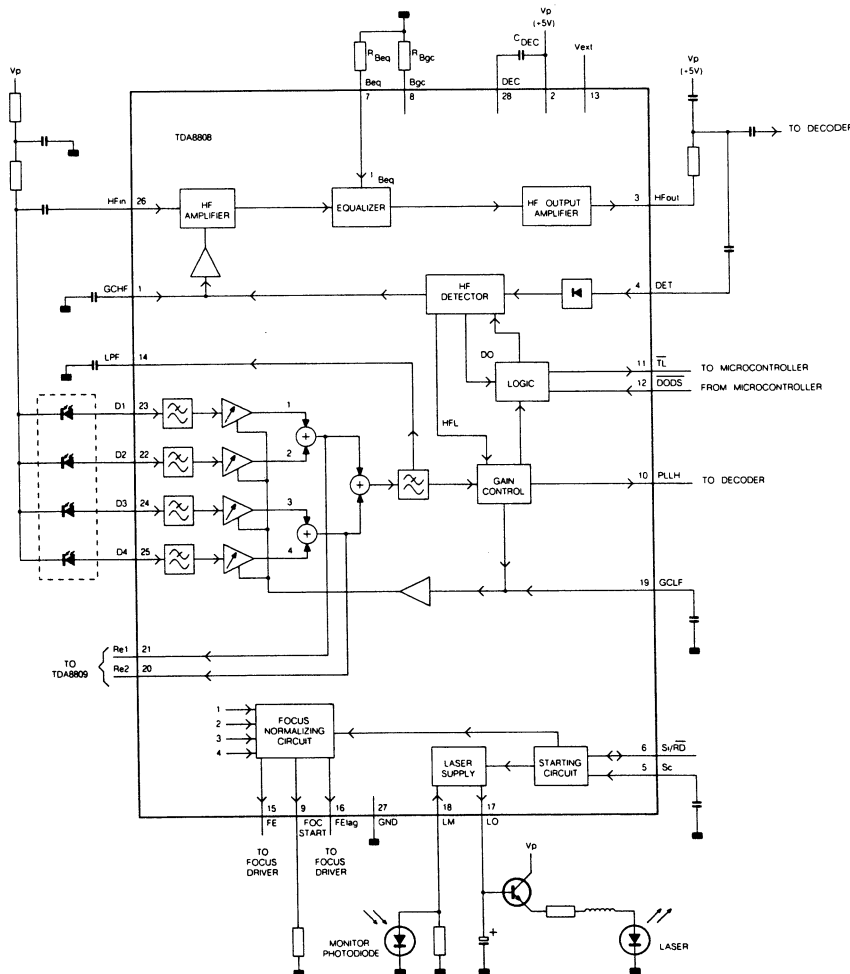
3.1.4.4 The stop procedure

The stop routine stops the turntable motor in a controlled way. This means that a number of stoppulses (168 msec. long) are given depending on the the disc startup time and the position of the arm on the disc. The focus is set off when the turntable has stopped : so during the stop procedure the motor is checked if it is still running, by means of Track Loss pulses.

**3.1.5 Photo Diode Signal Processor
TDA 8808 (item 7101)**

The TDA8808 is a bipolar integrated circuit designed for use in compact disc players with a single spot read out system. It amplifies the photo-diodes signals and processes the error signals for the focus- and radial control circuitry. Also built-in the laser supply, focusnormalizing circuit and focus starting circuit.

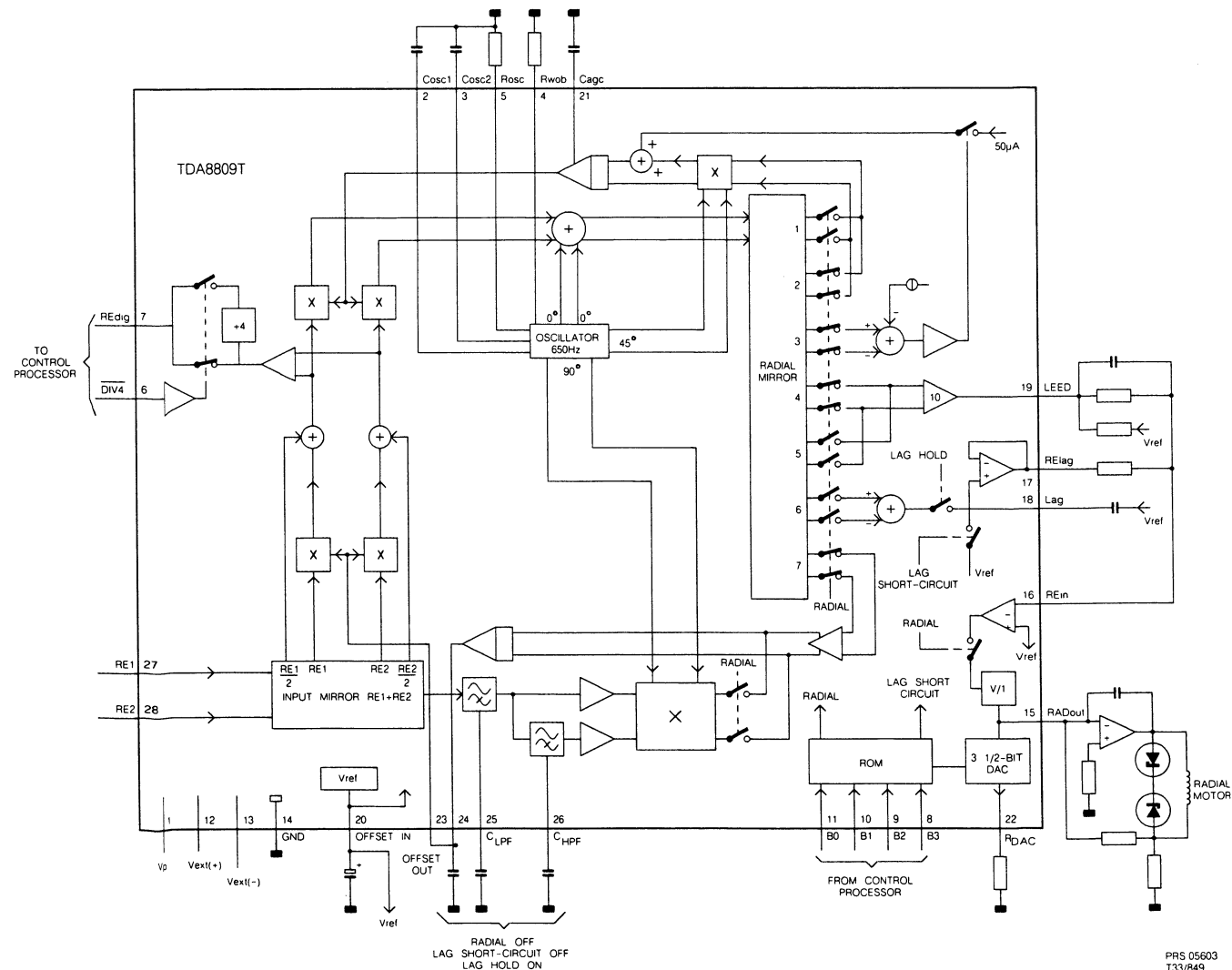
ABBREVIATION	PIN NBR	DESCRIPTION
DEC	28	Decoupling input (Internal bypass)
HF IN	26	HF current input to HF amplifier
D1 - D4	22 - 25	Current inputs to DC and LF photo diode amplifier.
RE1	21	Radial Error signal 1(summation of amplified currents D ₃ and D ₄ .)
RE2	20	Radial Error signal 2(summation of amplified currents D1 and D ₂ .)
GCLF	19	Gain control input for AC and LF amplifiers. Current output from LF amplitude detector.
LM	18	Laser Monitor diode input
LO	17	Laser amplifier current output
FE lag	16	Focus Error signal output for LAG network.
FE	15	Focus Error signal output.
CLPF (LPF)	14	Low Pass filter.
VBB (V _{ext})	13	Neg. Supply for FE and FE lag output stage.
DODS (DODS)	12	Drop Out Detection Suppression input
TL(TL)	11	Track Lost output
HFD(PLLH)	10	High Frequency Detector output
FS	9	Focus Start Focus normalizing circuit starting current.
BGC	8	DC and LF gain control ref.input.
BEQ	7	Equalizer reference current input.
(SI/RD)	6	On/Off control for laser supply and focus circuit. Ready Signal,starting up procedure succesful.
SC	5	Starting up capacitor input.
DET	4	HF detector voltage input.
HFout	3	HF amplifier and equalizer voltage output.
Vp	2	Positive supply voltage
GCHF	1	Gain Control input of HF amplifier Current output from HF amplitude detector



**3.1.6 Radial Error Signal Processor
TDA 8809 (item 7121)**

The TDA8809 is a bipolar integrated circuit which provides control signals for the radial swingarm of the CDM. These control signals are received from the TDA8808 and velocity control signals (jump to, pause) from the drive (control)processor.

ABBREVIATION	PIN NBR	DESCRIPTION
RE2	28	Input for amplified currents from photo diodes D ₃ and D ₄
RE1	27	Input for amplified currents from photo diodes D ₁ and D ₂
CHPF	26	High Pass Filter for RE1 and RE2
CLPF	25	Low Pass Filter for RE1 and RE2
Offset out	24	Radial offset control output
Offset in	23	Radial offset control input
RDAC	22	Current output for bias resistor
AGC	21	Automatic Gain Control for RE signal
LEAD	19	Lead output
Lag	18	Connection of integrator for (RE1 - RE2) input current
RElag	17	Voltage output of integrated (RE2 - RE1) input currents
RE1(RE in)	16	Radial Error Input
REO(REOut)	15	Current output of amplified (RE2 - RE1) input currents
B0 - B ₃	8 - 11	Input control bits for radial circuit
RP(REdig)	7	Digital output signal (RE2 - RE1)
DIV4(DIV4)	6	Divide by 4 input
Rosc	5	Biassing resistor for oscillator
Rwob	4	Wobble generator input
Cosc2	3	Frequency setting cap.for wobble osc.
Cosc1	2	
Vp	1	Positive supply voltage

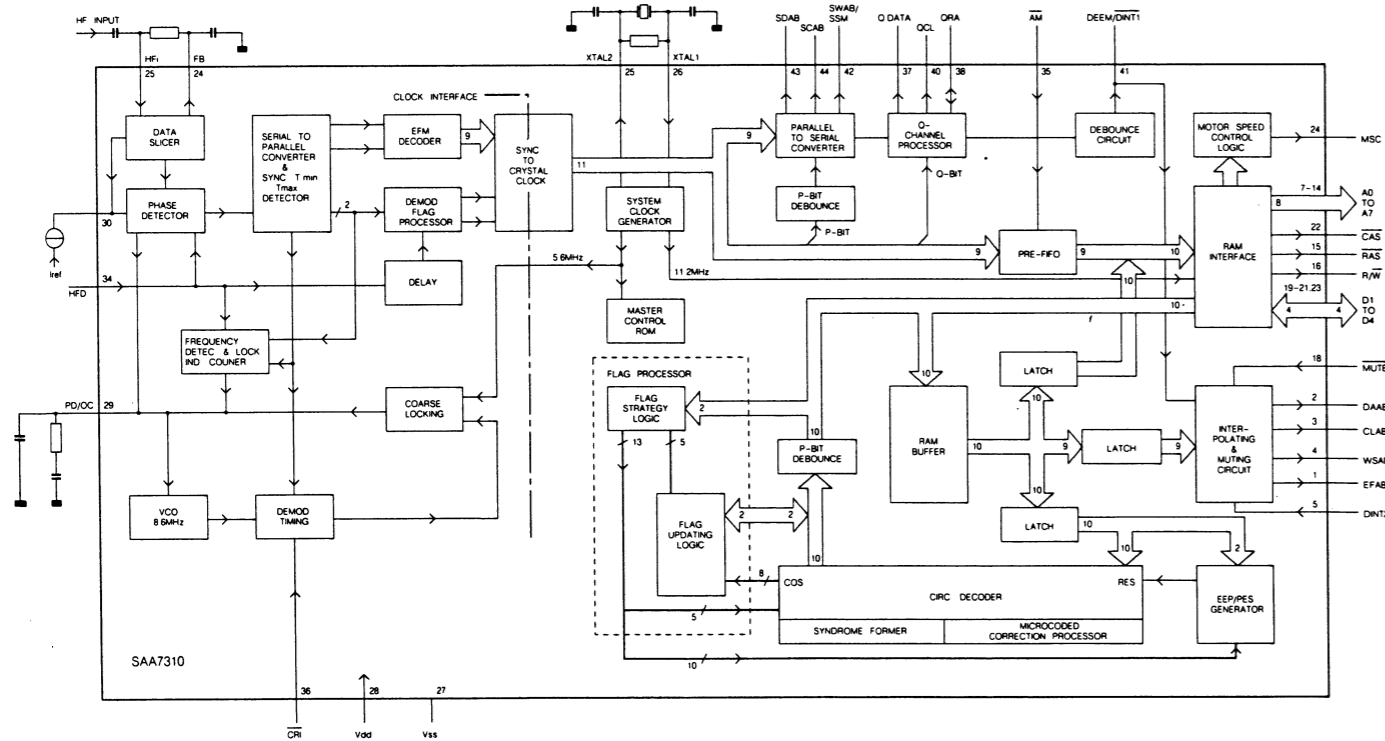


PRS 05603
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3.1.7 Decoder SAA 7310 (item 7301)

The SAA7310 incorporates the functions of demodulator, subcoding processor, error corrector and concealment in one CMOS chip.
 HF signal from the disc (EFM) is decoded and output as serial data to the ADOC IC (item 7310 on the CD panel)
 Also built-in the turntable motor speed control.

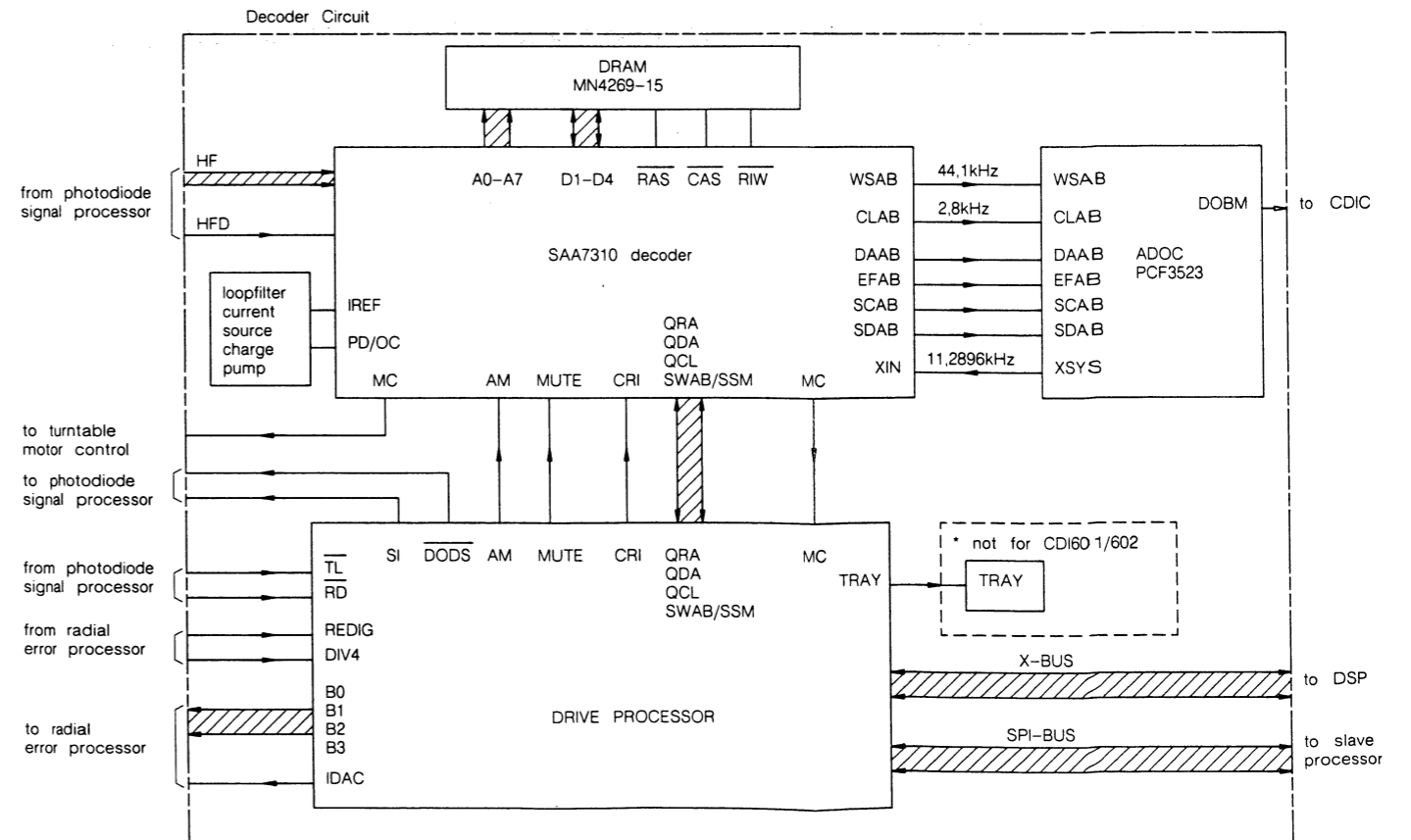
ABBREVIATION	PIN NBR	DESCRIPTION
EFAB	1	Error Flag output indicating data unreliable.
DAAB	2	Data output of I ² S bus
CLAB	3	Clock output of I ² S bus
WSAB	4	Word select output of I ² S bus
DINT2	5	Data Interpolated input
A0 - A ₇	7 - 14	Address outputs to Ext. RAM
RAS (RAS)	15	Row Address Select output to Ext.
R/W (R/W)	16	Read/Write output signal to Ext. RAM
MUTE(MUTE)	18	Mute signal input from μP.
D1 - D3	19 - 21	Data inputs / outputs to Ext. RAM
D4	23	Data input/output to Ext.RAM
CAS(CAS)	22	Column Address Select output to Ext.RAM
MC(MSC)	24	Motor Speed Control output.
XTAL2	25	Crystal output
XTAL1	26	Crystal Input
PD/OC	29	Phase Detector Output / Oscillator Control Input
CREF(Iref)	30	Current Reference Input.
FB	31	Feedback output.
HFI	32	High Frequency Input
HFD	34	High Frequency Detector
CRI(CRI)	36	Counter Reset Inhibit
QDA	37	Q-Channel Data signal output
QRA	38	Q-Channel Request input/Acknowledge output.
QCL	40	Q-Channel Clock input.
SWAB/SSM	42	Subcoding Word Clock output and Start/Stop Motor input
SDAB	43	Subcode Data output.
SCAB	44	Subcode Clock output.



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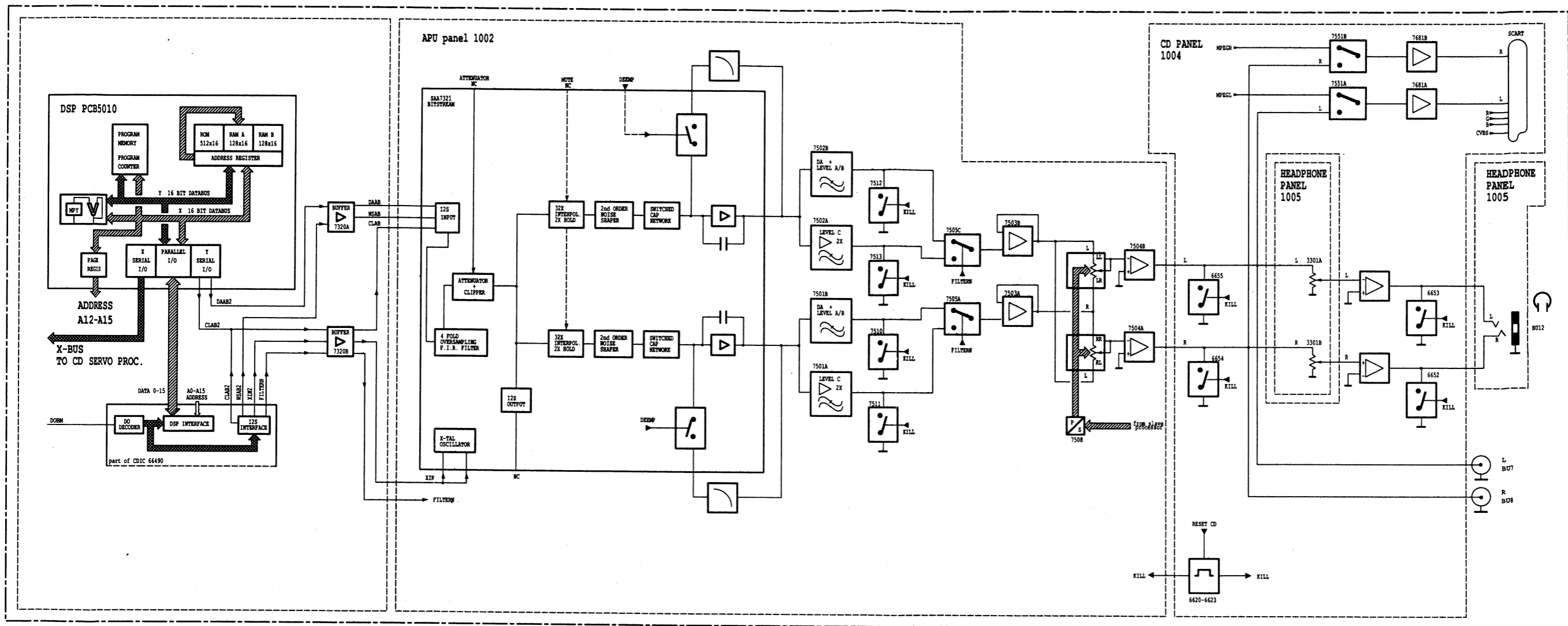
3.1.8 Audio Digital Output Circuit (ADOC) PCF3623 (item 7310)

ABBREVIATION	PIN NR.	DESCRIPTION
WSAB	1	Word Select Input of I ² S bus
CLAB	2	Clock Input of I ² S bus
DAAB	3	Data Input of I ² S bus
EFAB	4	Error Flag: Indicating unreliable data when HIGH. Copied to the validity bit in the DOBM output signal.
FS32(NC)	5	Sampling Frequency in channel status block : 44,1 KHz when this input is HIGH 32 KHz when LOW. This input has an internal pull-up.
SCAB	6	Subcode Clock input : 10 bit burst lock, which synchronizes subcode data.
SDAB	7	Subcode Data input : 10 bit burst data.
VSS	8	Ground : circuit earth potential.
XIN	9	Crystal oscillator input from crystal or slave clock
XOUT	10	Crystal clock drive output to clock crystal.
XSYS	11	System Clock output : 256 x Fs.
TESTB(NC)	12	Test input : HIGH for normal operation. This input has an internal pull-up.
DOBM	13	Digital Output Biphase Modulated signal
DOEN	14	Digital Output ENABLE : disables DOBM when LOW. This input has an internal pull-up.
ATSB(NC)	15	Attenuation : when LOW this input provides -12 dB attenuation. This input has an internal pullup.
VDD	16	Power supply input +5V



MDA 02928
HAS CDIDOC5

BLOCK DIAGRAM OF THE AUDIO PATH



3.2 Audio Part (Analog)

The complete audio circuit (digital and analog parts) is situated on two main boards: the CD panel and the MMC panel, and on two sub-panels: the APU (Audio Processing Unit) and the headphone panel.

The high-frequency information is read from the disc, decoded in the CD-3A decoder (SAA7310) and transformed by the ADOC chip (PCF3523) into a serial data stream D.O. (This D.O. signal is described in the CD-DA standard as Digital Audio Interface for domestic use).

These two chips (CD-3A decoder and ADOC) are located on the CD panel.

The D.O. signal is sent to the CD interface circuit on the MMC panel.

The heart of the CD interface consists of the CDIC (IMS66490) and the digital signal processor PCB5010. The CDIC, as part of this CD interface, divides the DO signal into Audio data and non-Audio data (e.g. data for Video chip set).

The non-audio data are routed under the control of the main uP (68000 bus).

The audio data is processed by the CDIC in case of CD-DA, and is decoded together with the DSP in case of ADPCM.

The generated signal as output of the CD interface is in accordance with the I2S format and is routed to the APU panel.

There the digital information is converted into a real analogue audio signal.

This is performed by our single bit D/A convertor SAA7321. Additionally, volume control and mixing take place for CDI applications. The L and R audio signals are available on BU-7 (L) and BU-8 (R) as well as on the headphone socket (BU 12).

3.2.1 APU Panel (Audio Processing Unit).

See block diagram CDIdoc6

The APU processes the data obtained from the CD interface.

The APU panel converts this digital audio information into the analogue audio signals L and R. Moreover, two other audio operations take place on this panel: the volume control and a mixer circuit. The following key components are located on the APU: SAA 7321, a single-bit DAC which is sometimes also called bit stream D/A convertor, and two dual R-2R ladder network DAC's which act as attenuator/mixer circuit.

3.2.1.1 Single-Bit DAC (bit stream) SAA7321 (Item 7400)

PIN NO.	ABBREVIATION	DESCRIPTION
1	CDR	Capacitor Damping Right
2	DER	De-Emphasis Right
3	VrefR	Reference voltage Right
4	VSSAR	Ground Analogue Right
5	VSSA	Ground logic Analogue section
6	VSSAL	Ground Analogue Left
7	VrefL	Reference voltage Left
8	DEL	De-Emphasis Left
9	CDL	Capacitor Damping Left
10	INTL	Integrator Left
11	VDDAL	Power Supply +5V Analogue Left
12	OALI-	Operational Amplifier Left Input-
13	OALI+	OpAmp Left Input+
14	OALO	OpAmp Left Output
15	VDDref	Power Supply: +5V
16	VRO	Reference Voltage Output
17	VRC	Reference Voltage Capacitor
18	TEST4	Test output 5 (NC)
19	DAO	I2S Serial Data Output (NC)
20	CLO	I2S Serial bit Clock Output (NC)
21	WSO	I2S Word Select Output (NC)
22	VDD1	Power supply +5V Digital
23	VDD2	Power Supply +5V (OSC)
24	XTAL2	Crystal oscillator output
25	XTAL1	Crystal oscillator input
26	XSYS	System clock output (NC)
27,28	VSS	Ground digital section
29	TEST1	Test input 1
30	WSI	I2S Word Select Input (WSAB)
31	CLI	I2S Serial bit Clock Input (CLAB)
32	DAI	I2S Serial Data Input (DAAB)
33	n.c.	
34	DEC	De-Emphasis Control
35	MUTE	Mute:
36	ATT	Attenuation
37,38	TEST2,3	Test output 2 and 3 (open)
39	VDDA	Power Supply +5V Analogue
40	OARO	OpAmp Right Output
41	OARI+	OpAmp Right Input +
42	OARI-	OpAmp Right Input -
43	VDDAR	Power Supply +5V Analogue right
44	INTR	Integrator Right

The data presented to the inputs of the APU either comes from CD-DA tracks or from CD-I tracks, but in both cases it has the I²S or Inter IC Soudp format. See fig. MDA 00648.

The serial digital information (DAAB), together with the clock signal (CLAB) and the corresponding synchronisation signal for the Left and Right channels (WSAB), is supplied, via print connector A016, to pins 30, 31 and 32 of IC 7400 (SAA 7321).

During the conversion from digital to analogue the digital samples are first converted into a high-speed 1-bit data stream, which is used by a 1-bit DAC for the actual conversion to the analogue signal.

The main functions in the 1-bit data stream D/A conversion are:

- Digital filtering and oversampling (256 x in all)
- Noise shaping and code conversion to 1-bit data stream.
- 1-Bit switch capacitor network as 1-bit DAC.

The conversion signal path is shown in the block diagram of IC 7400. The DAC is followed by third-order low-pass filters for left and right, which are used for filtering the higher frequencies that are produced during the conversion. These filters are built around IC 7501A-B and 7502A-B.

For CD-DA the 16-bit sample is oversampled 256x in all. Thus, with a sample frequency of 44.1 KHz, a 1-bit data stream is obtained of:

$$44100 \times 4 \times 2 \times 32 = 11,2896 \text{ MHz.}$$

This is the system clock frequency (XIN), which is presented via plug A023, pin 2, to pins 24 and 25.

Typical I²S signal forms are shown in figure MDA 00648. The corresponding time base applies to CD-DA. For the data corresponding with the CD-I audio data information other time bases hold. (See test instructions APU steps 3 - 4.)

The information for the A - B - C levels is transmitted with a different system clock frequency (XIN).

This (XIN) is dependent on the original sampling frequency. The output level of IC 7400 is dependent on this clock frequency. For level C the output level must be compensated.

In addition to the filter function, an amplifier has been built around IC 7501A and 7502A for level C. Gain factor: 2x. For CD-DA and the A and B levels no amplitude compensation takes place. The switch-over is effected by the FILTERN signal, which is generated in the CDIC on the MMC panel.

This signal is presented, via connector A016 pin 7, to pins 9 and 10 of electronic switches IC 7507 A and C.

The outputs of these electronic switches are supplied to the attenuator/mixer circuit via voltage follower IC 7503 A and B for the R and L channels.

Both audio channels are fed to both DAC's IC 7506 and IC 7507, which organize the volume control and the mixing of audio L and R. For CD-DA the attenuator is switched off and the channels for Left and Right are passed on 1:1. For CD-I audio the setting of the attenuator/mixer is dependent on the application. The commands for this, originating from the slave processor on the MMC panel, are presented serially via A011 to IC 7508, where they are converted into parallel data (D0 ÷ D7).

The AD 7528 contains two identical 8-bit D/A converters: DAC a and DAC b. Each DAC consists of an inverting R-2R ladder network with 8 weighted bit switches. In this way a binary- weighted current, which is dependent on the bit switches switched on, is obtained at the output.

3.2.1.2 Dual 8-bit DAC AD7528 Item 7506/7507

PIN NO.	ABBREVIATION	DESCRIPTION
1	Agnd	Ground (Analog)
2	OutA	Output DAC A
3	RFBA	
4	VrefA	Input DAC A
5	DGND	Ground (digital)
6	DAC A/B Control input	DAC A or B
7:14	DB7:DB0	Data inputs DB7(MSB)-DB0(LSB)
15	CS	Chip select input (active low)
16	WR	Write mode input (active low)
17	VDD	Power supply +5V
18	VrefB	Input DAC B
19	RFB B	
20	OUT B	Output DAC B

Then the L and R channels, whether or not attenuated and/or mixed, are fed to IC 7504 A and B, where current-to-voltage conversion takes place, and are then fed in amplified form to the CD panel via print connector A009.

3.2.2 Audio circuit on CD panel.

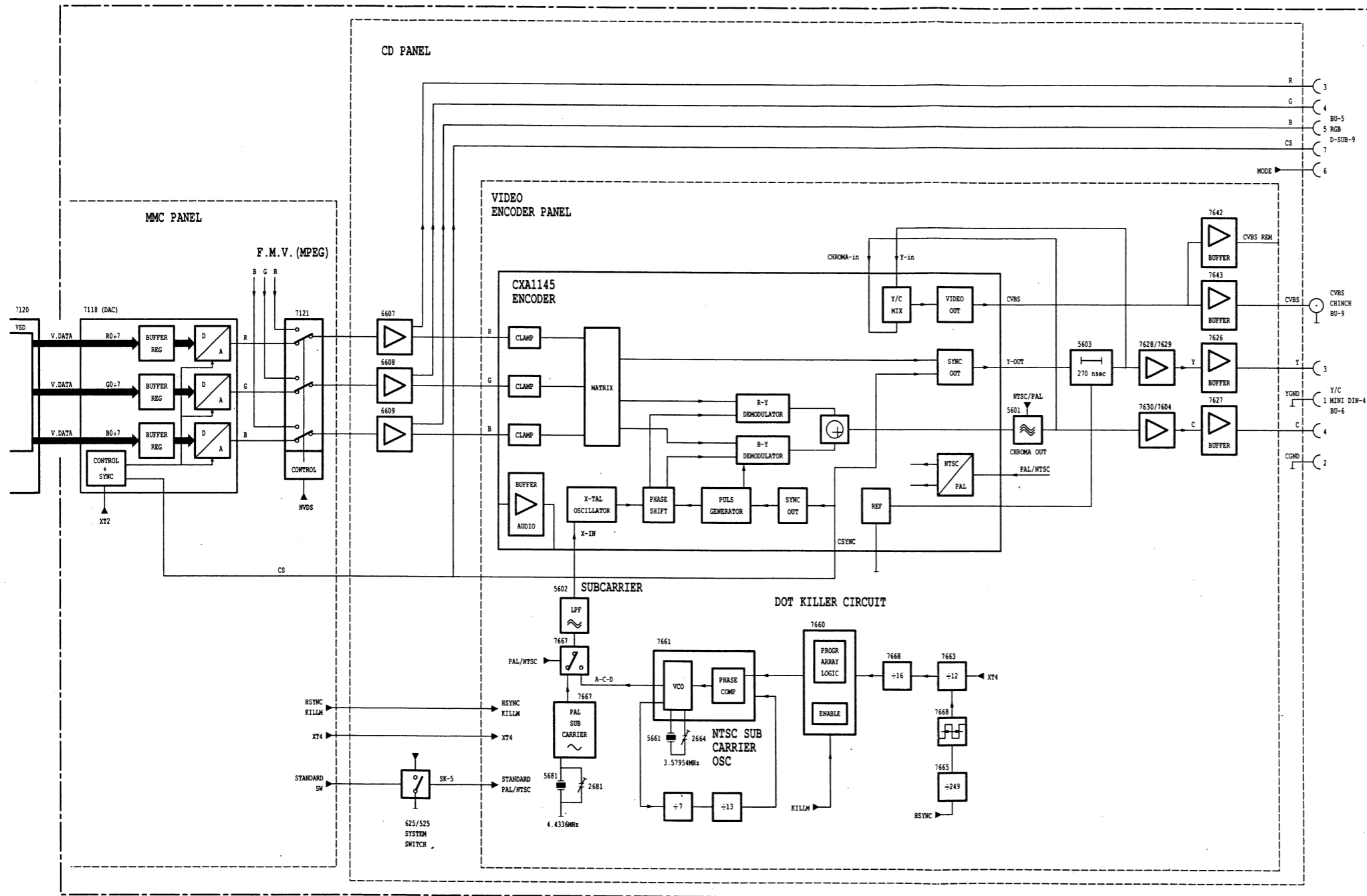
See Block diagram CDIdoc6

On the CD panel the audio signal is available at cinch connectors BU-7 and BU-8 for the L and R channels respectively.

The audio signals for the headphone output are first amplified again by IC 7561 A and B, which are also located on the CD panel.

The headphone volume control (3301) takes place on the headphone panel, which also accommodates the headphone connection(BU-12). Moreover, a mute signal is generated from the RESETCD signal for the whole audio circuit. This signal is called KILL and operates the mute switches 7510 ÷ 7513 on the APU panel (via connector A025 pin 6) as well as the mute switches 6652 ÷ 6655 on the CD panel. The mute switches prevent interference at the audio outputs during reset caused by energy discharges of electrolytic capacitors in the audio circuit.

BLOCK DIAGRAM OF THE VIDEO PATH



3.3 Video Part (See block diagram cdi doc 11)

The analog signals for R-G-B as video information are available at the outputs of the DAC's in the VSR on the MMC panel.

They are fed, via buffers 6101 - 6102 - 6103, to the CD panel.

($\pm 1.4 V_{pp} / 75 \Omega$) There they are buffered (6607 + 6608) and presented to BU-5 (D-Sub-9), the output connector for R-G-B.

($0.7 V_{pp} / 75 \Omega$)

In buffers 6607 - 6608 - 6609, the R-G-B signals are also coupled out for the video encoder. ($\pm 1 V_{pp}$)

The corresponding horizontal and vertical synchronisation signals are also generated in the VSR and are available as the Composite Synchronisation signal (CSYNC). This signal is first buffered and then presented via 6104 to the CD panel.

There the signal is split up for the video encoder panel and for the R-G-B output connector. (BU - 5)

The video encoder panel is mounted on the CD panel via print connectors E1061 and E1062.

3.3.1 Video encoder panel

On the video encoder panel, the following video output signals are generated from the analog R-G-B video information and the CSync signal:

- CVBS (Colour Video Blanking Signal)
- Y/C or S-Video.

The video signals (R-G-B) and the corresponding timing signals

(CSync and HSync), originating from the MMC panel, are presented via the CD panel to the video encoder panel.

In addition to the signals above, which are needed for the video encoder, the auxiliary signals KILLM - XT4 and SW are presented via the CD panel.

The necessary subcarriers for modulation of the chroma signals are generated on the encoder panel. Two reference oscillators have been added for this. For the PAL standard a crystal oscillator suffices. For the NTSC standard a PLL circuit consisting of a VCO, a phase discriminator and a dot killer circuit has been mounted.

3.3.1.1 PLL circuit (NTSC only)

The NTSC standard also enables non-interlaced video to be processed. (524 lines). With CVBS, a dot pattern may appear in the coloured parts of the image. This is not desirable for the many still pictures that are used in CD-I. Therefore the dot killer circuit has been mounted. This circuit is only functional if the NTSC standard has been selected.

The PLL locks the NTSC subcarrier to the horizontal frequency which is derived from the system clock signal (XT4).

HSYNC is divided by 249 in IC 7665, resulting in a signal with a repetition frequency of 63,18 Hz ($15734 \text{ Hz} / 249$).

In IC 7668, the pulse width of this signal is changed from 64 μSec to 133nsec. This pulse prevents IC 7663 from

counting at the same frequency.

This results in a 63,18 Hz offset on the system clock signal (XT4), causing the annoying dot pattern to disappear in case of non-interlaced video.

In IC 7663, XT4 is divided by 12, taking account of the detuning that is introduced by the pulse at pin 10 of IC 7663. The terminal count pin 15 is connected through to IC 7668, where XT4 is divided by 16. (see also the circuit diagram)

As a result XT4 has been divided by 192 ($12 \cdot 16$), with or without an offset, depending on the level of the enable signal KILLM (KILLM=active low) at pin 1 of connector E 1063.

The output signal at pin 13 of IC 7668 has a frequency of 39335 Hz and a 50% duty cycle. Via the other path, the subcarrier frequency generated by the VCO is divided by 91, namely by 13 in IC 7662 and by 7 in IC 7664. This signal is also added to the Phase Locked Loop and also has a frequency of 39335 Hz. Consequently, the subcarrier frequency is locked to XT4.

3.3.1.2 Encoder

Among the components that are located on the video encoder panel is **Video encoder CXA1145P (Item 7601)**.

PIN NO.	ABBREVIATION	DESCRIPTION
1	GND1	Ground
2	RIN)	Inputs for Analog RGB
3	GIN)	
4	BIN)	
5	XO-out	NC
6	XO-in	Input for subcarrier
7	NTSC/PAL IN	Input for NTSC/PAL mode
8	Audio in	NC
9	Audio out NC	
10	C sync in	Input for composite sync signal
11	C sync	NC
12	VCC1	Power Supply: +5V
13	I Ref	Ref. current
14	V Ref	Ref. Voltage
15	CHROMAO	Chroma signal output
16	Yout	Luminance signal output
17	CHROMAI	Chroma signal input(BPF)
18	Yin	Luminance signal input (delay time)
19	VCC2	Power Supply: +5V (RGB+CVBS outputs)
20	Cvideo O	Composite video output (CVBS)
21	Bout)	Outputs for Analog RGB
22	G out)	
23	R out)	
24	GND2	GND (RGB + CVBS output)

The level of SW defines the standard, NTSC or PAL, at the encoder output. If this signal is "high" (+ 5V), the system operates in the NTSC mode, if it is low, the system operates in PAL.

The frequency of the subcarrier at the input (Xin) of the encoder is determined by means of switch IC 7667, blocks A and C. If SW is high, the frequency at Xin (pin 6 of IC 7601) is 3.579MHz; if SW is low, the frequency is 4.433 MHz. The circuit around 5602 is a low-pass filter.

The other inputs for encoder IC 7601 are: R,G,B & CS (Composite Sync). From these signals the luminance signal (Y), to which the CSYNC is added in the ADDER, is obtained in the matrix. The colour difference signals R-Y and B-Y are obtained by modulation. The C (chroma) is composed by the adder circuit. The Chroma signal is sent through a bandpass filter around 5601, which can be switched over for the two different standards. The difference in delay for the luminance signal (Y) is compensated in delay line 5603. Both signals are amplified and buffered, enabling them to be loaded with 75 Ohms. This takes place in 7628/7629 and 7626 for the Luminance signal and in 7603/7604 and 7627 for the Chrominance signal.

These signals are furthermore connected to the IC, Yin and Chroma in respectively, which mixes them in a matrix, thus producing the CVBS signal. (Composite Video & Blanking Signal).

This signal is buffered (7643) and output, after which it is available via the CD Panel on the CVBS terminal BU-9.

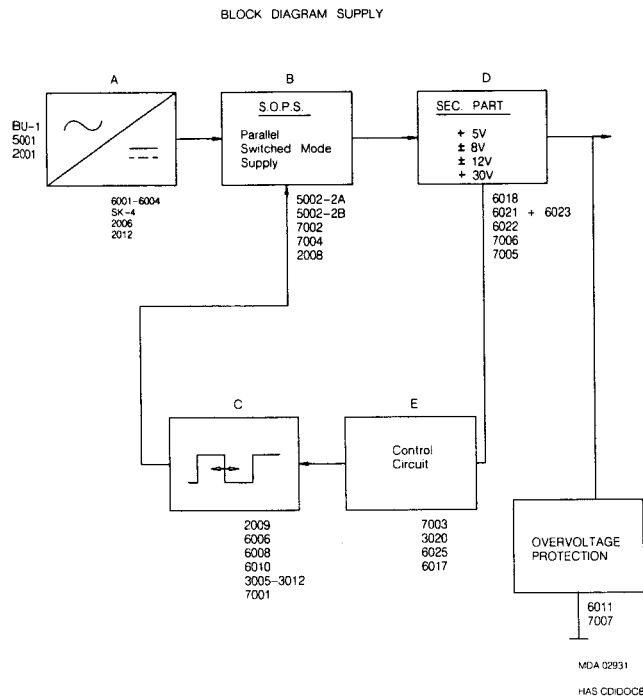
The signal is also available for versions having a remodulator.

3.4 The Power Supply (SOPS) Part

The abbreviation SOPS stands for Self Oscillating Parallel Switched Mode.

The SOPS is a mains-isolated power supply and is suitable for mains voltages of 96-132 Vac and 198-264 Vac.

The output voltages are: +30V, +/-12V, +/-8V and 5V. The power supply can handle powers between 13 and 55W, provided that the 5V is loaded with at least 1.5 A. The apparatus is protected against overloads and short-circuits at the outputs.



The power supply can be divided into 5 blocks:

Block A comprises the mains filter, the primary rectifier and smoothing circuit, which, depending on the mains voltage range selected, acts as a Graetz rectifier or as a voltage doubler; in both cases a nominal direct voltage of abt. 300 V is obtained.

Block B comprises the transformer with the control circuit.

Block C comprises the parts which constitute the pulse-width modulator.

Block D comprises the secondary rectifier with additional filtering for the sampling frequencies.

Block E comprises the control circuit, which can influence the pulse-width modulator via the optocoupler.

3.4.1 Principle of operation

The power supply works according to a discontinuous flyback principle, in which the energy consumed by the transformer 5002 during the conduction of switching transistor 7002 is completely dissipated via the secondary windings during the "off" time.

The "on" time of the switching transistor is determined by the pulse-width modulator.

The "off" time is determined by the output voltage, the load and the preceding "on" time. At the end of the degaussing phase the voltages on the windings are reversed again, causing the voltage across auxiliary winding 1-3 of transformer 5002 to activate the switch again.

Immediately after the switch-on of the power supply the switching transistor is activated by starting resistor 3002 and capacitor C2008 is charged a little. As soon as the base-emitter threshold is exceeded, 7002 will start conducting.

As the auxiliary winding is wound in the same sense as the main winding 7-6 of transformer 5002, a small voltage drop across this winding will also increase the base drive via winding 1-3, so that switching transistor 7002 is completely switched through. At the same time, 2009 is charged via 6010.

After a short period the voltage across 2009 reaches the threshold voltage of 7001, causing switching transistor 7002 to be cut-off. The voltages on the transformer are reversed and the energy is dissipated via the secondary windings until the transformer is completely degaussed. At the end of this phase the voltages are reversed again, so that the switch is activated again.

3.4.2 The pulse-width modulator

The pulse width depends on:

- the timer elements 2009, 3005, 3006 and 6017
- the mains voltage via auxiliary winding 1-3 and diode 6006
- the output voltage via the optocoupler (fine adjustment)
- the output voltage via auxiliary winding 1-2.

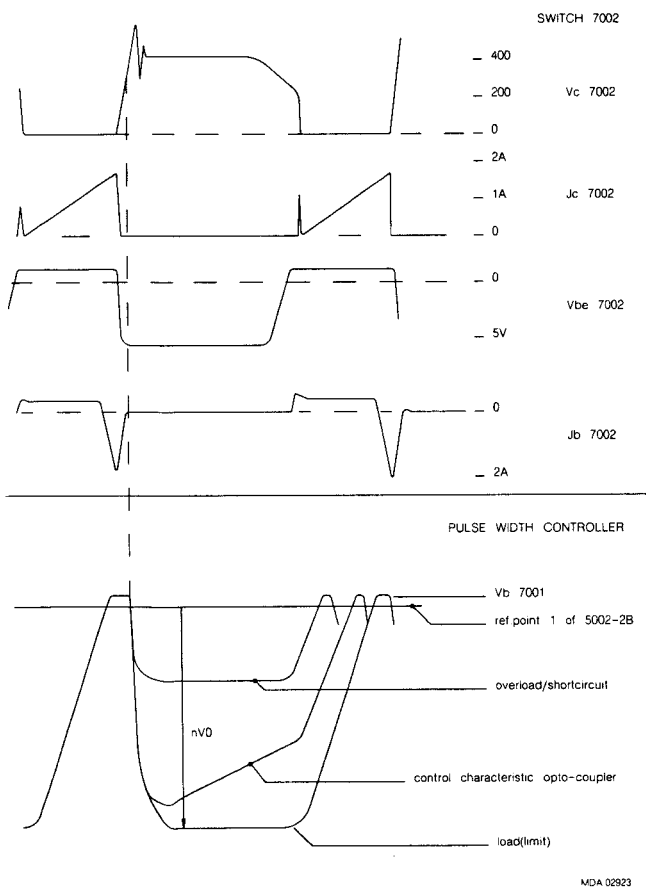
Re a. After the switch-off of transistor 7002, the timer capacitor, when functioning normally, is discharged via 3007, 6008 and winding 1-2 to a negative voltage relative to the emitter of 7001. The voltage across this winding is a measure for the output voltage and thus is more or less constant. In the conducting state of the switching transistor the capacitor is charged via 6006, 3006, 3005 and 6017 to a voltage that is determined by winding 1-3. When V_{BE} is reached, 7001 will start conducting, cutting off the switching transistor.

Re b. As the charging takes place in the conducting phase of the switching transformer, the voltage across winding 1-3 will vary in proportion to

the mains voltage. At a high mains voltage, capacitor 2009 will be charged more quickly and the switching time will become shorter, and vice versa.

Re c. A stable output voltage is effected by the control circuit. The charge time of capacitor 2009 is affected via the optocoupler.

Re d. As the capacitor is discharged by the voltage across winding 1-2, which is a measure for the output voltage, a soft-start function will be obtained during the switch-on phase, as a result of the slow growth of the output voltage, and a fold-back characteristic will be obtained in case of an overload or short-circuit, as a result of the failure of the output voltage.



3.4.3 Control circuit

The control circuit (block E) takes care that the 5.2 V output voltage remains constant. The other output voltages are coupled so well that they are practically independent of load variations. A reference voltage, obtained from the 12V output, is applied to the base of 7003 where it is compared with the 5.2 V output voltage. If the 5.2 V voltage increases, 7003 will start conducting more. This control information is transferred by the optocoupler to the primary side. Consequently, capacitor 2009 is charged more quickly, so that 7002 is switched off sooner and thus less energy is transferred.

3.4.4 Overvoltage protection

For the protection of the IC set of the player, the 5.2 V output is protected against overvoltage. This circuit is adjusted at 6.2V +/- 0.5 V. If the voltage across 3024 exceeds a value of 2.5V, 6011 will start conducting and in turn will pull 7007 into conduction. As a result the voltages will be reduced considerably and a clearly audible bleep will occur.

The cause of the overvoltage protection being energized, must be looked for in the control circuit.

Servicing hints :

The power supply has a few characteristic error conditions.

- * If, after a repair, the power supply is loaded with the specified load, a bleep will be audible between 10 and 50 Vac when the supply voltage is being turned on (starting of the power supply).
- * If the fuse is broken, one can be sure that the 7002 is also defective. Sometimes 7001 and 7004 will also be defective.
- * If the power supply produces a bleep, there are two possible error conditions:
 - a) a secondary short-circuit in the power supply or in the player.
 - b) the overvoltage protection has been energized.
- * If the overvoltage protection is energized, this is also noticeable from the fact that 7007 becomes hot. The error can be traced to a defect in the control circuit.

3.5 The Multi Media Controller (MMC part)

The MMC is the heart of the CD-I player, the circuitry can be divided into three blocks :

- Systemcontrol
- Audioprocessing
- Video & Subsystem

This section is only a review of the the main key components, which are used in the circuits.

The functioning of the the MMC part can be checked by built-in service software the so called Low-level test program. For more detail of the tests see the Service Manual section 5.

If there is a defect in one of the blocks then the complete MMC panel must be replaced and send for Central Repair (see Service Manual section 3.6).

3.5.1 Systemcontrol

The systemcontrol hardware consists of:

- * Master C.P.U.
- * Slave C.P.U.
- * System ROM
- * NV-RAM + Timer-clock
- * Clock circuit

3.5.1.1 Master C.P.U.

As master c.p.u. is used the SCC68070, a 16/32-Bit microprocessor. The master c.p.u. runs the CD-RTOS software modules.

The SCC68070 also includes a UART interface, which is connected to PORT 2 of the player. To determine the proper functioning of the basic blocks directly, the Low-level test is used via this UART interface.

For more information on features and operation of this microprocessor refer to the "User Manual, Part1 - Hardware" of the SCC68070.

3.5.1.2 Slave C.P.U.

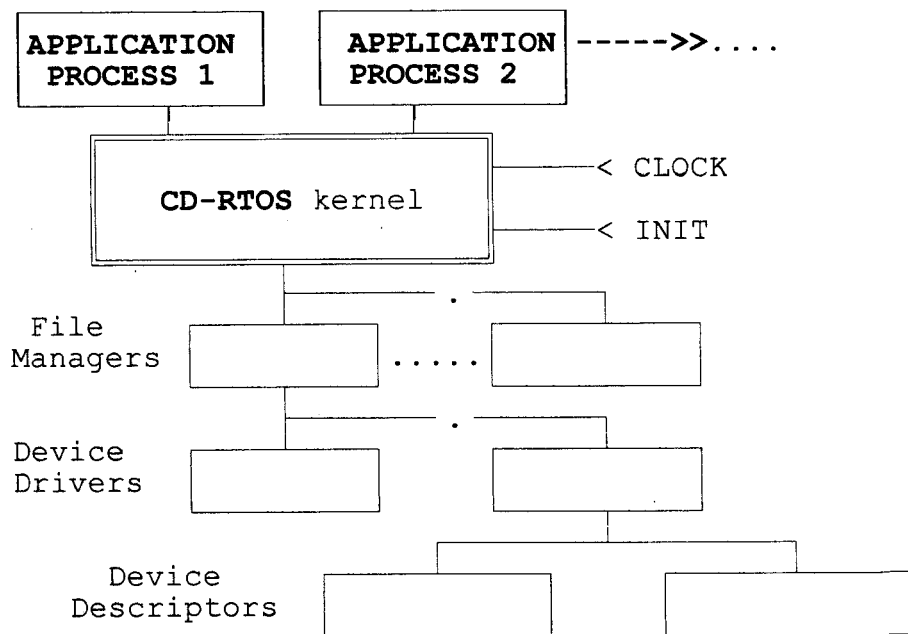
This microprocessor controls port #1, RC5 decoding and attenuation of the audio output.

The slave is checking continously if a device is present at port #1 and will send this information to the Master. So it is possible to change input devices during operation (mouse/tablet). Information from the remote control joystick and pointing device on port #1 is combined by the slave processor and sent to the Master. If the Master CPU is communicating with the CD processor via the SPI bus , the Slave is put in the transparant mode.

3.5.1.3 System ROM

All CD-RTOS (Compact Disc Real Time Operating System) software modules, User Shell data, Service Shell data and other system data are stored in the system Read Only Memory.

3.5.1.3.1 CD-RTOS software



The kernel is the central system manager. It decides which process is to be executed, grants memory to processes on request and handles other requests by processes. I/O calls are passed on to a file manager/device driver.

A file manager controls a group of related devices and is a hardware independent module. Each file manager may support multiple device drivers ; a device driver performs direct hardware control. A driver is written for specific hardware but can control multiple instances of that hardware. The device descriptor describes one single instance of a device and contains only data (like base address, device driver & file manager name for example).

The clock module makes sure the kernel gets control every 10 msec. If the clock circuitry or clock module does not work, multi processing is not possible. The init module describes some parameters of the whole system (like name of the console device).

3.5.1.4 NV-Ram + Timer Clock

NV-ram and Timer clock are integrated into one chip. In the NV-ram personal (game-)results, playershell settings, FTS data and CSD (Configuration Status Description) files are stored.

The Timer clock controls the calendar/time function. In the terminal Low level test an adjustment of this timer function is provided in step 11. (For more details see the Service Manual section 5.1.6)

3.5.1.5 Clock circuit

System clock : 30.0000 Mhz (for PAL)
30.2098 Mhz (for NTSC)
UART clock : 4.9152 Mhz
Slave clock : 4.00 Mhz

3.5.2 Audioprocessing

The key components of the audioprocessing part are:

- * CDIC (Compact Disc Interface Circuit)
with external S RAM
- * DSP (Digital Signal Processor)

3.5.2.1 CDIC

The CDIC interfaces the CD part and the MMC part. The Digital Output is processed with the DSP in case of audio and then send via the IIS interface output to the APU. On-chip :

- * CD-player Interface
- * SRAM Address generator
- * IIS interface
- * I/O controller SRAM/System bus
- * Parallel I/O for DSP

3.5.2.2 DSP

The main function of the DSP is :

- * Decoding ADPCM sound data
- * Generating serial PCM data (IIS)
- * Send commands to CD-driver via X-bus, like:
 - Start/Stop/Pause
 - GOTO /Jump

In case of CD-DA the DSP is in the .Transparent mode.

3.5.3 Video & Subsystem

This part consists of :

- * Master VSC (Video and System Controller)
with external DRAM bank 0
- * Slave VSC
with external DRAM bank 1
- * VSD (Video Synthesizer)
with external Triple DACs for RGB
videosignals

3.5.3.1 VSC's (Master...Slave)

The main functions of the two VSC's are:

- * Transferring pixel data from system bus into
 - Display data
 - Video timing signals
- * DRAM controller
- * System controller
- * Shared memory (total 1 Mbyte) for:
 - Video pixel data
 - Program data (CD-I disc)
 - System data (CD-RTOS)
 - Sound Maps

3.5.3.2 VSD with external DACs

This device combines input from both VSC's into one image. The main functions are:

- * Generating analog RGB signals from display data of VSC's
- * Overlaying video planes like :
 - Curser
 - Foreground 1
 - Foreground 2
 - Background
- * Providing special Effects on images like:
 - Dissolve/ Fading
 - Mosaics
- * Providing special visual effects on images by programming
 - Partial updates
 - Wipes
 - Curtains
 - Blinds
 - Squares

THE MMC PANEL

